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# OPTIMIZATION OF GaN-on-Si HEMTs FOR HIGH VOLTAGE APPLICATIONS

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*To my grandparents*

*Nonno Gianni & Nonna Mimma*

"(...) your work is going to fill a large part of your life,
and the only way to be truly satisfied is to do what you believe is great work.
And the only way to do great work is to love what you do.

(...) don`t be trapped by dogma.
Don`t let the noise of others` opinions drown out your own inner voice.
And most important, have the courage to follow your hearth and intuition. They
somehow already know what you truly want to become."

*Steve Jobs, Stanford 2005*

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Leuven 2011

# Abstract

This Ph.D. thesis focuses on the optimization of GaN-on-Si high electron mobility transistors (HEMTs) for high voltage applications. We optimized devices based on AlGaN/GaN/AlGaN double heterostructures (DHFET) for achieving high breakdown voltage. Two identical breakdown mechanisms are identified in both epilayer buffer structure and devices. For devices with short gate-drain distance, the breakdown voltage linearly increases with the gate-drain distance being dependent on the device geometry. More specifically, it is dependent on the electric field peak at the gate edge on the drain side. Indeed, the experimental implementation of an optimized field plate increases the breakdown voltage by more than a factor two. For devices with long gate-drain distance, the device breakdown voltage saturates at a value determined by the nitride buffer layer thickness. Indeed, the increase of the buffer layer thickness allows higher saturated breakdown voltage. The field plate improves the saturated breakdown voltage by only 10%. Importantly, this behavior is found even if the Si substrate is highly resistive. The breakdown voltage is also measured with the Si substrate grounded. The value obtained is a factor two lower than the value measured with the Si substrate floating. Therefore, due to the higher conductivity of Si compared to the III-nitride layers, leakage current flows from the ohmic contacts into the substrate and along the Si interface. High voltage simulations of AlGaN/GaN transistors with and without Si substrate qualitatively confirm the electrical measurements. The simulations of AlGaN/GaN/Si heterostructures with different gate-drain distance show the saturation of the breakdown voltage due to the high impact ionization factor at the Si interface. Due to the lower critical electric field of Si, the structure breaks at the Si interface where the electric field is not homogeneously distributed due to the roughness of the Si interface. Therefore, we can conclude that the limiting factor of GaN based transistors fabricated on buffer layer grown on Si substrate for high voltage applications is the Si substrate itself. Therefore, for GaN-on-Si transistors, to make the breakdown voltage linearly increase with the gate-drain distance and to eliminate the saturation, we use the Si trench around the drain contact technique in order to break the horizontal leakage path at the Si interface.

# Korte samenvatting

Deze doctoraatsthesis handelt over de optimalisatie van GaN-op-Si transistoren voor hoogvermogen toepassingen. Om een hoge doorslagspanning te realiseren werden transistoren gebaseerd op AlGaN/GaN/AlGaN-dubbele heterostructuren geoptimaliseerd. Het doorslagmechanisme voor zowel de bufferlaag als de transistor is identiek. Voor een korte afstand tussen de poort en de afvoer schaalt de doorslagspanning evenredig met deze afstand. In dit geval wordt de doorslagspanning bepaald door de grootte van het elektrisch veld bij het einde van de poort aan de afvoerzijde. Door verbinding van een gemetalliseerde veldplaat met de poort kan de doorslagspanning met een factor twee worden verbeterd. In het geval van een grote afstand tussen de poort en de afvoer daarentegen verzadigt de doorslagspanning bij een waarde welke bepaald wordt door de dikte van de nitride bufferlaag bovenop het Si-substraat. Dit gedrag is onafhankelijk van het doperingsgehalte van het Si-substraat: dezelfde saturatiewaarde wordt gemeten voor Si-substraten met een hoge weerstand. In dit verzadigingsregime kan de doorslagspanning slechts met 10 percent worden verbeterd door het gebruik van een veldplaat. De doorslagspanning werd ook gemeten met een geaard Si-substraat. In dit geval is de doorslagspanning een factor twee kleiner vergeleken met een vlottend Si-substraat. Door de hogere geleidbaarheid van het Si-substraat vergeleken met de III-nitride bufferlaag, vloeit de lekstroom van het Ohmse contact naar het substraat en dan langs het substraat grensvlak. Bij hoge spanning breekt de transistor in het Si-substraat omwille van het lagere kritisch veld van dit materiaal vergeleken met III-nitrides. Om deze reden concluderen we dat het Si-substraat de limiterende factor is voor het bereiken van een hoge doorslagspanning voor GaN-op-Si transistoren. Hoogspanningsmodellen voor AlGaN/GaN-transistoren, zowel met als zonder aanwezigheid van het Si-substraat, werden opgesteld en de resultaten zijn in qualitatieve overeenstemming met de elektrische metingen. De berekeningen tonen een verzadiging van de doorslagspanning bij grote poort-afvoer afstanden door de hoge impactionisatie aan het Si-grensvlak. Om het probleem van de beperking van de doorslagspanning door aanwending van Si-substraten op te lossen, wordt voorgesteld om het lekpad aan het grensvlak te onderbreken door het lokaal etsen van Si-grachten omheen de afvoer.

# List of publications

## Journal contributions

1. **D. Visalli**, M. Van Hove, P. Srivastava, D. Marcon, K. Geens, X. Kang, E. Vandenplas, J. Viaene, M. Leys, K. Cheng, B. Sijmus, S. Decoutere and G. Borghs, "GaN-on-Si for high voltage applications", *The Electrochemical Society Transactions, vol. 41, issue 8, p. 101, 2011.*

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Tested in Off-State at a Record Drain Voltage of 200V and 200°C", *Japanese Journal of Applied Physics, vol. 49, no. 4. p. 04DF07-1, 2009.*

## Conference contributions

1. **D. Visalli (invited speaker)**, M. Van Hove, P. Srivastava, D. Marcon, K. Geens, X. Kang, E. Vandenplas, J. Viaene, M. Leys, K. Cheng, B. Sijmus, S. Decoutere and G. Borghs, "GaN-on-Si for high voltage applications", *220$^{th}$ Electrochemical Society Meeting, October 9-14, Boston (Massachusetts), 2011.*

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# Table of Contents

# List of symbols

| Symbol | Description | Units |
|---|---|---|
| $A$ | Active device area | $m^2$ |
| $a_0$ | Lattice constant | Å |
| $c_0$ | Height of the hexagonal lattice cell | Å |
| $C_{13}$, $C_{33}$ | Elastic constant | Pa |
| $\Delta E_C$ | AlGaN/GaN conduction band offset | eV |
| $\varepsilon$ | Relative dielectric constant | |
| $e_{31}$, $e_{33}$ | Piezoelectric constants | $C/m^2$ |
| $E_c$ | Conduction band | eV |
| $E_{crit}$ | Critical electric field | V/m |
| $E_D$ | AlGaN surface state energy | eV |
| $E_F$ | Fermi level | eV |
| $E_G$ | Band gap energy | eV |
| $E_{G\_AlGaN}$ | Band gap energy of AlGaN | eV |
| $E_P$ | Electric field due to the polarization | V/m |
| $I_{DS}$ | Source-drain current | A |
| $I_{DSS}$ | Saturated source-drain current | A |
| $L_{FP}$ | Field plate length | m |
| $L_G$ | Gate length | m |
| $L_{GD}$ | Gate-drain distance | m |
| $L_{SD}$ | Source-drain distance | m |

| Symbol | Description | Units |
|---|---|---|
| $L_{SG}$ | Source-gate distance | m |
| $\mu_n$ | Electron mobility | $cm^2/V{\cdot}s$ |
| $n_s$ | 2DEG sheet carrier concentration | $m^{-2}$ |
| $P_{pe}$ | Piezoelectric polarization | $C/m^2$ |
| $P_{sp}$ | Spontaneous polarization | $C/m^2$ |
| q | Elementary charge | C |
| $R_{ON}$ | On-resistance | Ω |
| $R_{ON}A$ | Specific on-resistance | $\Omega{\cdot}m^2$ |
| $\sigma_{2DEG}$ | 2DEG charge density | $m^{-2}$ |
| $\sigma_{pol}$ | Polarization sheet charge density | $m^{-2}$ |
| $\sigma_{surf}$ | Surface charge density | $m^{-2}$ |
| $t_{CR}$ | Critical AlGaN thickness | m |
| $V_{BD}$ | Breakdown voltage | V |
| $V_{DS}$ | Drain-source voltage | V |
| $V_{GS}$ | Gate-source voltage | V |
| $V_{Ga}$ | Gallium vacancy | |
| $V_N$ | Nitrogen vacancy | |
| $V_T$ | Threshold voltage | V |
| W | Device width | m |

# List of acronyms

| Acronym | Description |
|---|---|
| 2DEG | Two dimensional electron gas |
| BHM | Baliga's figure of merit for high frequency |
| BM | Baliga's figure of merit for low frequency |
| CMOS | Complementary metal-oxide semiconductor |
| CZ | Czochralski Si substrate |
| DD | Drift diffusion model |
| DG | Density gradient model |
| DHFET | Double heterostructure |
| EPC | Efficient power conversion corporation |
| FET | Field effect transistor |
| FIB | Focused ion beam |
| FP | Field plate |
| FZ | Float zone Si substrate |
| GTO | Gate turn-off thyristor |
| HD | Hydrodynamic model |
| HEMT | High electron mobility transistor |
| IC | Integrated circuit |
| ICP-RIE | Inductive coupled plasma reactive ions etching |
| IGBT | Insulator gate bipolar transistor |
| IT | Information technology |

| Acronym | Description |
|---|---|
| I-V | Current-Voltage characteristic |
| JM | Johnson's figure of merit |
| KM | Keyes' figure of merit |
| LED | Light emitting diode |
| MET1 | Sample with mesa etching time of 1 minute |
| MET5 | Sample with mesa etching time of 5 minute |
| MET10 | Sample with mesa etching time of 10 minute |
| MBE | Molecular beam epitaxy |
| MIS | Metal insulator semiconductor |
| MOCVD | Metal organic chemical vapor deposition |
| MOSFET | Metal oxide semiconductor field effect transistor |
| NL | Nucleation layer |
| PV | Photovoltaic |
| RF | Radio frequency |
| SHFET | Single heterostructure |
| SJ-MOS | Super junction metal oxide semiconductor |
| SRP | Spreading resistance probe |
| TEM | Transmission electron microscopy |
| UPC | Uninterruptible power systems |

# Chapter 1

# Introduction

In the past few years, Gallium Nitride (GaN) has attracted much attention due to several advantages over Silicon (Si) such as large band gap energy, high critical electric field, high electron mobility, high saturation drift velocity and melting point. In 1991, Nakamura *et al.* presented the first high brightness GaN-based blue LED with an output power ten times higher than the conventional Silicon Carbide (SiC) blue LED.[1] Since then, GaN technology has rapidly diffused in the optoelectronic applications.[2] However, to be a commercially viable technology, the main requirement is low cost. This is only possible by growing GaN on top of large diameter Si substrate. With the successful growth of GaN on top of Si despite the large lattice and thermal mismatch, GaN-on-Si technology has emerged as the best alternative to the well established but aged Si technology.[3,4] In 2009, GaN-on-Si technology started diffusing in several applications such as RF power amplifier.[5] This has opened the door to the diffusion of this technology in high voltage power switching applications[6]. Recently, Efficient Power Conversion Corporation (EPC) has launched its second generation of enhancement-mode GaN power transistors on 150 mm Si substrate with a drain-source voltage of 200 V and a maximum on-resistance of 25 mΩ with 5 V applied to the gate contact (eGaN®FET).[6] Compared to a state-of-the-art silicon power metal-oxide-semiconductor field-effect transistor (MOSFET) with similar on-resistance, the eGaN®FET is much smaller and has many times superior switching performance. Several applications benefit from eGaN®FET performance such as high-speed DC-DC

power supplies, notebook and netbook computers, telecom base-stations and cell phones.[6] Despite the fact that the GaN technology has broken into the market, it is still behind its theoretical performance.[7]

When this Ph.D. work started only a few groups were studying the behaviour of GaN-on-Si devices at high voltage. However, a detailed study about the breakdown mechanisms was lacking. This work is the first detailed study of the breakdown mechanisms of GaN-on-Si devices where the impact of the Si substrate is identified and addressed.

In this chapter, we will first discuss the main performance requirements of high voltage switching devices. Then, we will analyze the advantages of using GaN compared to other materials in terms of material properties and figures of merit. Also, an overview of the application areas and of the state-of-the-art of the GaN-on-Si devices is discussed. Finally, we will describe the organization of this thesis.

## 1.1 Performance required for high voltage switching devices

In the field of electric power conversion, transistors should behave as an ideal switch. High breakdown voltage and low energy losses are the most important requirements. The energy losses of a switching device are divided into static losses and dynamic losses. The static losses are the losses when the transistor is in the on-state and off-state. In the on-state a transistor should demonstrate very low on-resistance in order to decrease the conduction losses. In the off-state the transistor should behave as a perfect open but, inevitably, some residual current, leakage current, flows. This leakage current should be very low in order to reduce the standby power consumption. The switching losses are due to the capacitance and the switching from the on-state to the off-state and vice versa which should be fast. Another requirement for the switching transistors is related to the passive elements such as capacitances, inductances and filters which form the power conversion system. By increasing the operation frequency, it is possible to reduce the size of the passive elements used, which results in a size reduction of the power conversion system. Therefore, the higher operation frequency is required as an important specification of a switching device. The operation frequency of the main silicon power switching devices such as gate turn-off thyristor (GTO) and insulated gate

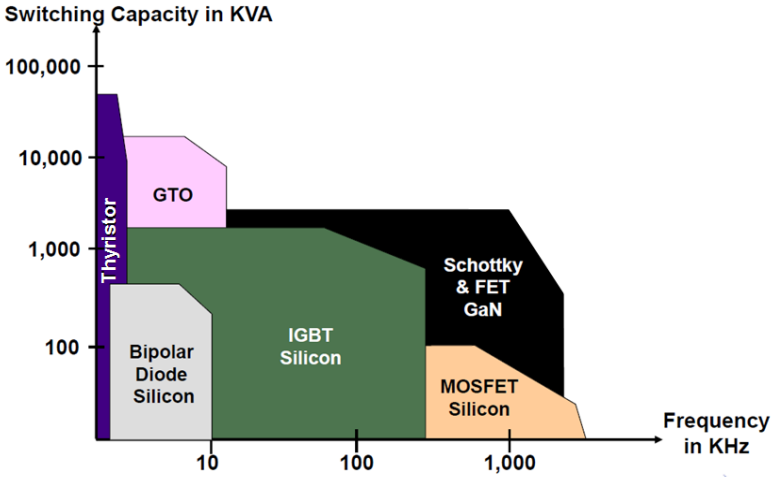


**Fig. 1.1** Overview of the switching capacity as function of the operation frequency for different device categories[7].

bipolar transistor (IGBT) is only in the range between Hz and kHz while GaN and Si MOSFET devices can handle several MHz. The GaN technology not only extends the operational frequency of the silicon GTO and IGBT but also, very important, extends the switching capacity of the MOSFET devices as shown in Fig. 1.1.[7] Finally, the requirements for an electric power switching device can be summarized as follows:

- High blocking voltage, which expands the utilization field;
- Low specific on-resistance, which reduces the device conduction losses;
- Low capacitance, which reduces the switching losses and increases the operation frequency;
- High operation frequency, which reduces the apparatus size.

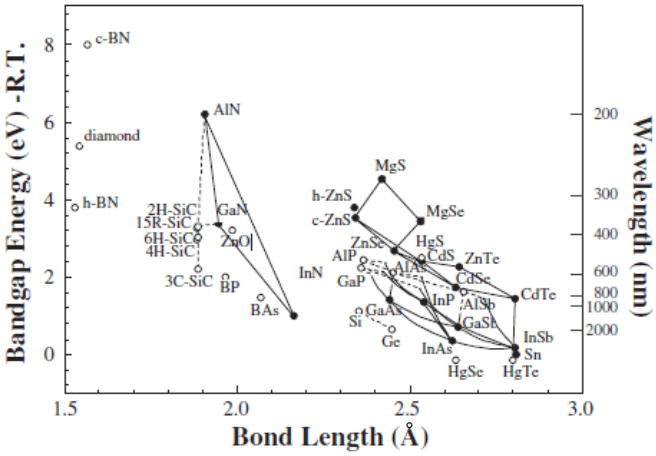


**Fig. 1.2** Relationship between bond length and band gap energy for various kinds of semiconductor materials.[8]

## 1.2 Advantages of AlGaN/GaN HEMTs as switching devices

### 1.2.1 GaN material properties

The fundamental properties of the III-N materials are the small bond length between constituent atoms and the wide bandgap energy. Figure 1.2 shows the relationship between the bond length and the bandgap energy of various kinds of semiconductors materials.[8] III-nitrides and SiC materials are located in a quite different plot area compared to other compound semiconductors. The small bond length leads to a strong bonding energy between constituent atoms and, consequently, the chemical stability is extremely high. In addition, the large bonding energy and the small mass bring about large phonon energy so lattice scattering hardly occurs. This results in high thermal conductivity and high saturation drift velocity, macroscopically. Moreover, the large bandgap leads to high breakdown electric field and low intrinsic carrier generation at high temperature. This allows high temperature operation without excessive leakage

current. These characteristics are extremely attractive for high-frequency, high-power, high-voltage, high-temperature and low-loss operating specifications.[8]

### 1.2.2 Comparison with other material systems

The main material properties of GaN compared to other semiconductors are reported in Table 1.1. A large bandgap results in high breakdown electric field which enables the application of high supply voltages. Also, it leads to low intrinsic carrier generation at high temperature. Both GaN and SiC have a very large band gap energy which results in a breakdown electric field ten times higher compared to Si and GaAs.

Generally, to achieve high currents and high frequency operation, high carrier mobility and high saturation velocity are desirable. GaAs shows the highest value of electron mobility. Indeed, the field-effect transistors (FETs) fabricated from this material have an excellent high-frequency performance. On the contrary, the disadvantage of fabricating transistors from bulk GaN and SiC is the low electron mobility which is 900 $cm^2\ V^{-1}\ s^{-1}$ and 400 $cm^2\ V^{-1}\ s^{-1}$, respectively. However, the ability of III-nitride materials to create a two dimensional electron gas (2DEG) at the heterointerface of an AlGaN/GaN device with high charge density and very high mobility compared to the value of the bulk GaN is the most important property of these materials. The AlGaN/GaN high electron mobility transistors (HEMTs) exhibit a 2DEG channel with a mobility between 1200-2000 $cm^2\ V^{-1}\ s^{-1}$ and a sheet carrier density of 1.0-1.5 $10^{13}\ cm^{-2}$. This is one of the reasons for which the AlGaN/GaN devices are preferred compared to the SiC devices. In Chapter 2 we will explain the formation of the 2DEG channel.

The thermal conductivity of a semiconductor material is extremely important since this parameter describes its ability to conduct heat. Poor values lead to device degradation at elevated temperatures. In general, conventional semiconductors are poor thermal conductors, in particular GaAs. Conversely, SiC is an excellent thermal conductor. GaN is comparable with Si, which is the best of the conventional semiconductors.

**Table 1.1** Physical properties of different semiconductors considered for high-voltage applications.[8]

| Material properties | Si | 6H-SiC | GaN | GaAs |
|---|---|---|---|---|
| Bandgap energy (eV) | 1.1 | 3.0 | 3.4 | 1.43 |
| Breakdown electric field (MV/cm) | 0.3 | 2.4 | 3.3 | 0.4 |
| Relative dielectric constant | 11.8 | 9.7 | 9.0 | 12.8 |
| Electron mobility ($cm^2\ V^{-1}\ s^{-1}$) | 1400 | 400 | 900<br>2000* | 8500<br>10000* |
| Saturated (peak) drift velocity ($10^7$ cm/s) | 1.0<br>(1.0) | 2.0<br>(2.0) | 2.5<br>(2.7) | 1.0<br>(2.1) |
| Thermal conductivity ($W\ cm^{-1}\ K^{-1}$) | 1.5 | 4.5 | 1.3 | 0.5 |

* values for the corresponding heterostructures

To finalize this paragraph, we can give a short summary about GaAs-, SiC- and GaN- technologies. GaAs devices have several drawbacks. Among them high substrate costs and low thermal conductivity are the most important. The latter makes it very difficult to remove heat when used in high-power applications. An additional drawback is the critical electric field which is much smaller than that of GaN. SiC technology has emerged in the past 10 years as the best choice to overcome the limits of the Si technology. SiC devices benefit from the excellent thermal conductivity of the substrate. However, their electron mobility is significantly lower than that of GaN devices due to the lack of heterojunction technology in this material. Moreover, SiC technology suffers from very high intrinsic material cost and is not highly scalable in substrate size, epitaxial deposition equipment throughput, material supply, and device-fabrication manufacturing platforms. Additionally, another disadvantage is the complexity of the processing. On the contrary, the cost of the GaN technology can be lowered by growing the III-nitride materials on a Si substrate which is available in large diameters up to 300 mm. From a processing point of view, GaN-on-Si devices can be processed in the Si high volume foundries using the same high throughput and high yielding process

**Table 1.2** Normalized figures of merit of wide bandgap semiconductors[8].

| FOM | Si | 6H-SiC | GaN | GaAs |
|---|---|---|---|---|
| JM ($E_c\, v_{sat}/2\pi$) | 1 | 260 | 760 | 7.1 |
| KM $\kappa(v_{sat}/\varepsilon)^{1/2}$ | 1 | 4.68 | 1.6 | 0.45 |
| BM ($\varepsilon\, \mu\, E_c^3$) | 1 | 110 | 650 | 15.6 |
| BHM ($\mu\, E_c^2$) | 1 | 16.9 | 77.8 | 10.8 |

technologies as used for Si-based devices. In Imec, we have recently demonstrated a fully CMOS-compatible GaN process on 200 mm Si substrates.[9]

### 1.2.3 Figures of merit

The figures of merit (FOM) combine the most relevant material properties, shown in Table 1.1, into a number which represents a rough measure of the relative strengths of the material with respect to high-power and high-frequency applications. These figures of merit are listed in Table 1.2 and more details can be found in the work of Baliga[3,10]. Here $\varepsilon$ is the relative dielectric constant, $\mu$ is the mobility, $E_c$ is the breakdown electric field, $v_{sat}$ is the saturated electron drift velocity and $\kappa$ is the thermal conductivity. JM is the Johnson's figure of merit defining a value for high-frequency handling capability. KM is the Keyes's figure of merit for high-temperature handling capability. Baliga derived two figures of merit, one for low and one for high frequency operations which are a measure of the high-power handling capability. As it is shown in Table 1.2, the SiC technology is a strong competitor of the GaN technology. In particular, in the applications where high temperature is required SiC is the best choice due to the higher thermal conductivity. Indeed, for some applications of the GaN technology, SiC is used as foreign substrate on top of which GaN is grown. However, this technology would be very expensive. For high frequency switching and high voltage applications, GaN

technology is superior due to the high saturation electron velocity, and the large bandgap and critical electric field, respectively. Based on Baliga`s work, from a material point of view, the best semiconductors for low and high-frequency power switching applications should exhibit large critical electric field and should have high carrier mobility.[3,10] Therefore, a significant performance improvement can be achieved by replacing Si with GaN.

### 1.2.4 Specific on-resistance $R_{ON}A$ versus breakdown voltage

Ideally, high values of breakdown voltage ($V_{BD}$) should be obtained with a low on-resistance ($R_{ON}$) but this is challenging because these two parameters are linked by a linear relation as shown from Eq. (1.1). Consequently, a trade-off must be found. For a vertical device structure with a uniform doping profile, the on-resistance of a FET may be calculated as:

$$R_{ON} = \frac{4\,V_{BD}^2}{\varepsilon \mu_n E_C^3} \quad \text{or} \quad \frac{V_{BD}^2}{R_{ON}} = \frac{\varepsilon \mu_n E_C^3}{4}. \tag{1.1}$$

The $V_{BD}^2/R_{ON}$ is called the power-device-figure-of-merit and the BHM was directly originated from this equation. As pointed out in Eq. (1.1), $R_{ON}$ rises with the square of $V_{BD}$. Hence, BHM defines the intrinsic limit of a power semiconductor. However, it was created for vertical FET structures only. An AlGaN/GaN HEMT is a lateral device and has different properties: the conductive channel is a two-dimensional charge and is not related to any doping in the material. Thus, it is necessary to derive a power-device-figure-of-merit for the AlGaN/GaN HEMTs. It is generally assumed that in an undoped GaN HEMT, the electrons in the channel are induced from the donor-like surface traps by the strong polarization field in the AlGaN layer and the surface is left positively charged by the empty traps, as explained in Chapter 2.[11] The 2-DEG density can be very high without intentional doping and its density depends only on aluminum composition.[12] Assuming a HEMT with gate width W, source to drain distance $L_{SD}$ and 2-DEG density $n_s$, the channel resistance is given by:

$$R = \frac{L_{DS}}{q\mu_n W n_s}\ [\Omega] \text{ or for specific on-resistance } R_{ON}A = \frac{L_{DS}^2}{q\mu_n n_s}\ [\Omega \cdot cm^2]. \tag{1.2}$$

In the lateral AlGaN/GaN HEMT, the total electric field ($E_{tot}$) is given by the vertical electric field due to the polarization ($E_p$) and by the lateral electric field due to the drain bias ($E_x=V_{DS}/L$) where L is the depletion region. At the breakdown, the gate-drain region is fully depleted and $E_x=V_{BD}/L_{GD}$ and $E_{tot}$ is the critical electric field of the AlGaN barrier layer, thus, $E_{tot} = E_{crit} = \sqrt{E_p^2 + E_x^2}$. Together with Eq. 1.2 and $L_{GD} \equiv L_{DS}$, the on-resistance can be expressed as

$$R_{ON} = \frac{V_{BD}^2}{q\mu_n n_s (E_{crit}^2 - E_p^2)}. \tag{1.3}$$

Equation 1.3 states that also for a GaN HEMT the on-resistance follows a square law with the breakdown voltage. The power-device-figure-of-merit established for a Si FET can be also applied to GaN HEMTs, which makes it possible to directly compare GaN HEMTs with other power devices. The only problem is that the 2DEG density $n_S$ in Eq. 1.3 is not a material parameter. The specific on-resistance in GaN HEMTs can be lowered by increasing the 2DEG concentration. This can be done by increasing the Al content of the AlGaN barrier layer. Since the critical field of AlGaN is also a linear extrapolation of that of GaN and AlN, we can relate $n_S$ to $E_{crit}$ directly as $q \cdot n_S = \zeta \cdot E_{crit}$ where $\zeta$ is a constant with a unit of [F/cm]. Therefore, Eq. (1.3) can be expressed as[13]:

$$\frac{V_{BD}^2}{R_{ON}} = \zeta \mu_n E_{crit} \left( E_{crit}^2 - E_p^2 \right). \tag{1.4}$$

Equation (1.4) is now in the same form as Eq. 1.1 for vertical Si and SiC devices. Due to the higher electric field and electron mobility it is easy to understand the enormous advantage of using a GaN-based device compared to a SiC-based device and, in particular, a Si-based device. Figure 1.3 shows the specific on-resistance calculated in Si, SiC and GaN power semiconductors. Most of the data published for the Si MOSFETs are clearly close to the theoretical limit. The early GaN commercial devices clearly show that AlGaN/GaN HEMTs are capable of delivering a breakdown voltage and on-resistance beyond the material limits of Si and SiC semiconductors used today for high-power switching applications.[14]

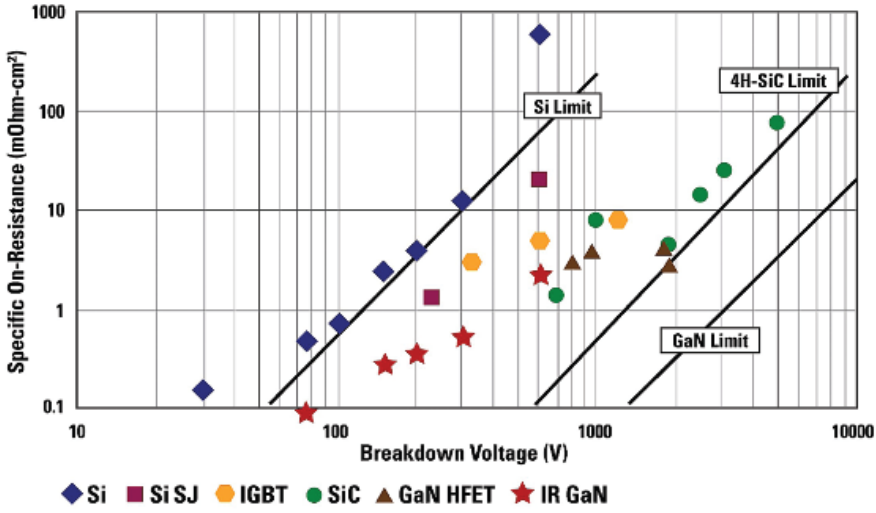


**Fig. 1.3** Specific on-resistance of GaN-on-Si based HEMTs and Si and SiC power MOSFETs.[14]

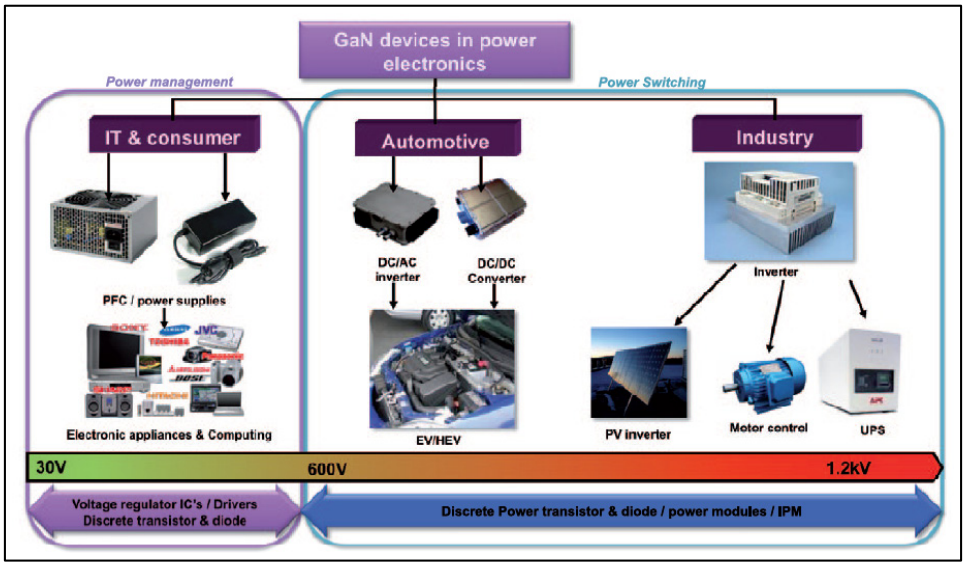


**Fig. 1.4** Possible applications for GaN devices in power electronics.[7]

## 1.3 Applications of high-voltage AlGaN/GaN switching HEMTs

GaN is a well implemented and widely used semiconductor technology in the LED optoelectronics industry[2]. For about 10 years, GaN devices have also been developed for RF wireless applications where they can replace Si transistors in some selected systems.[5] Since then, GaN technology is diffusing in the power electronic applications as well.[6] In the last 40 years, power electronics have been developed using Si devices such as MOSFET, GTO and IGBT. However, as shown in Fig. 1.3, these Si devices have approached their theoretical limits due to their own material properties. As we have discussed, compared to Si, GaN exhibits largely better figures for most of the key specifications such as critical electric field, bandgap energy and electron mobility. Intrinsically, GaN could offer a better performance compared to Si in terms of breakdown voltage, switching frequency and overall system efficiency. Nowadays, GaN technology offers transistors, diodes and even IC`s compatible with power electronic expectations, at least in the 0-600 V range. According to Yole Développement[7], the most

promising applications for nitride semiconductors would be IT and consumer, automotive and industry (PV inverters, UPS and motor control) as shown in Fig. 1.4. Today, about 67 % of the power electronics market is looking at the 0-900 V range and GaN-on-Si appears as the most cost effective solution. It has been calculated that GaN-on-Si HEMT could be 50 % cheaper than a SiC device with the same performance.

## 1.4 Research background of GaN-on-Si

When we started this work, in 2007, only a few reports about AlGaN/GaN HEMTs grown on Si for high-voltage applications were presented in the literature. The main problem in this technology is the large lattice and thermal mismatch between Si and III-nitride layers which cause several type electrical active defects affecting the device performance. In 2005 Arulkumaran *et al.*[15] reported on AlGaN/GaN devices with a breakdown voltage of 243 V and specific on-resistance as low as 0.47 $m\Omega \cdot cm^2$. They grew a thick AlN nucleation layer (NL) on top of Si followed by a thick GaN/AlN superlattice. They showed that the enhancement of the device performance with the increase of the AlN NL thickness is due to the reduction of electrically active defects at the Si interface. Hikita *et al.*[16] showed a GaN/AlN superlattice buffer with source-via grounding structure. They connected the source to the conductive Si substrate through a via-hole. Thus, the Si substrate acts as a backside field plate reducing the electric field at the gate edge. These devices showed a breakdown voltage as high as 350 V and a specific on-resistance as low as 1.9 $m\Omega \cdot cm^2$. In 2006, Choi *et al.*[17] grew a 1.4 µm thick GaN buffer layer with Fe doping to compensate the unintentional doping of residual impurities such as Si and O. They achieved a breakdown voltage as high as 195 V, 225 V and 295 V for a gate-drain distance of 5, 7 and 10 µm, respectively. The specific on-resistance was 1.42, 1.81 and 2.44 $m\Omega \cdot cm^2$, respectively. The Furukawa Electric company claimed that to increase the breakdown voltage it is necessary to compensate the unintentionally n-type doping of the GaN buffer layer by using a p-type dopant. They showed that the increase of the C concentration up to $8.0 \cdot 10^{18}$ $cm^{-3}$ makes the buffer breakdown voltage to increase. They achieved a device breakdown voltage as high as 518 V with a specific on-resistance of 3 $m\Omega \cdot cm^2$.[18] They also investigated different buffer structures for the growth of a high quality AlGaN/GaN heterostructure. They claimed that the use of three AlN (50nm)/two thick GaN (200 nm) buffer structure

lowers the threading dislocations and helps in the increase of the breakdown voltage.[19] In 2007, Iwakami *et al.*[20,21] showed devices with 800 V as breakdown voltage and 2.5 mΩ·cm$^2$ as specific on-resistance by using a 5.3 µm thick buffer layer with a thick GaN/AlN superlattice. Based on these results, for reaching high breakdown voltage GaN-on-Si devices thick buffer layer structures are required. Since the growth of a thick buffer layer on Si is quite challenging due to the large lattice and thermal mismatch people use the superlattice structure for a better stress control.

## 1.5 Synopsis of the thesis

This thesis focuses on the optimization of GaN-on-Si HEMTs for high voltage applications. After a brief description of the device physics of an AlGaN/GaN heterostructure presented in Chapter 2, Chapter 3 describes the optimization of this structure by performing TCAD simulations. In particular, the optimization of the AlGaN/GaN/AlGaN double heterostructure (DHFET) in terms of GaN channel thickness and Al content of the AlGaN buffer layer is presented.

Chapter 4 describes the device fabrication and the measurement configurations. We briefly describe the PowerSwitch mask, dedicated for the high voltage characterization. Then, the description of the processing with particular attention to the isolation step follows. Finally, the measurement configurations of the breakdown voltage in both vertical and horizontal directions and of the on-resistance are shown.

Chapter 5 summarizes the optimization of the nitride buffer structure grown on Si. We identified and addressed the breakdown mechanisms of the buffer structure. The impact of different isolations, epilayer thicknesses and Al content of the nitride buffer structure on the breakdown voltage are discussed.

Chapter 6 studies the behaviour of the GaN based devices at high voltage. The impact of the buffer thickness on the device breakdown voltage is investigated. Moreover, the simulations performed at high voltage perfectly match the experimental behaviour observed before and after removal of the Silicon substrate. Finally, an approach to the enhancement-mode devices is presented.

In Chapter 7, we study the origin of the parasitic leakage current bump detected in the leakage current in both buffer and device. The optical and electrical behaviour is investigated. We will also show an investigation on the AlN/Si interface performed by ESR.

Finally, Chapter 8 gives summary and conclusions of this Ph.D. work and an outlook for future research.

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# Chapter 2

# AlGaN/GaN High Electron Mobility Transistors on Si substrate

This chapter describes the physical properties of the AlGaN/GaN High Electron Mobility Transistor (HEMT). It starts with a short discussion about the substrates on which the III-nitride materials can be grown. As we already stated in the previous chapter, we grow our AlGaN/GaN HEMTs on a Silicon substrate in order to lower the cost of the GaN technology. Then, the crystal structure and the basic physical properties of such devices are discussed. Particular attention will be given to the piezoelectricity of these materials which is responsible for the formation of the two dimensional electron gas (2DEG) at the heterointerface. The Imec *in-situ* SiN passivation technique is shown to enhance the 2DEG characteristics, such as carrier concentration, mobility and sheet resistance. Finally, an analysis of the bulk, surface and interface defects in GaN with a description of the current collapse phenomena is presented.

**Table 2.1** Comparison of substrate properties. The lattice and thermal mismatch is calculated with respect to GaN.

| Substrate Properties | Si (111) | $Al_2O_3$ (100) | 6H-SiC | GaN (0001) |
|---|---|---|---|---|
| Lattice constant (Å) | 3.846 | 4.758 | 3.081 | 3.189 |
| Lattice mismatch (%) | -17 | -33 | 3.5 | - |
| Thermal expansion coefficient ($10^{-6}$ $K^{-1}$) | 2.6 | 7.3 | 4.5 | 5.6 |
| Thermal mismatch (%) | 116 | -23 | 24 | - |
| Thermal conductivity (W $cm^{-1}$ $K^{-1}$) | 1.5 | 0.5 | 4.5 | 1.3 |
| Wafer size | 2”→12” | 2”→8” | 2”→6” | 2” |
| Price | low | medium | very high | extremely high |

## 2.1 Substrate issues

Ideally III-nitride materials would be grown on a native substrate but, as it is very difficult to synthesize them, they are available only in small size and their cost is extremely high. Therefore, they are grown on foreign substrates such as sapphire ($Al_2O_3$), silicon carbide (SiC) and silicon (Si). The properties of these substrates are listed in Table 2.1. The lattice and thermal mismatch is calculated with respect to the GaN material. Traditionally, sapphire is the most commonly used substrate. It is semi-insulating, can withstand the required high growth temperatures and is relatively cheap. However, sapphire is not suitable for high-power applications due to the very low thermal conductivity. SiC shows better substrate properties such as high thermal conductivity and low thermal and lattice mismatch. These are the reasons for the better quality of the GaN layers grown on top of it. However, the SiC substrates are very expensive. They are mostly employed for the fabrication of HEMTs for microwave applications where high thermal conductivity is needed. Silicon as substrate is very attractive due to the very low cost and large size availability. Recently, we have

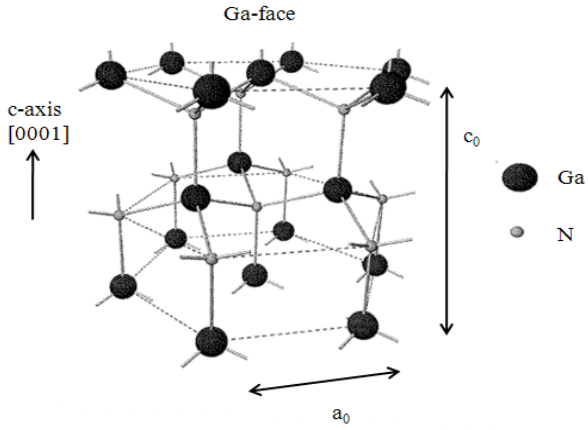


**Fig. 2.1** Atomic arrangement in Ga-face GaN crystal. $C_0$ is the height of the hexagonal lattice cell and $a_0$ is the lattice constant.

successfully demonstrated the growth of high quality GaN on 150 mm and 200 mm Si substrate.[1,2] However, the large lattice mismatch between GaN and Si leads to a large number of defects which could affect the device performance[3]. Moreover, the large thermal mismatch (116%) could lead to a severe wafer bowing or layer cracking, which makes the growth of thick GaN buffer layer very difficult. Details of the growth of III-nitrides on Si are discussed by Cheng.[4]

## 2.2 GaN material system

### 2.2.1 Crystal structure

The group of III-nitride, AlN, GaN and InN, can crystallize in three crystal structures: wurtzite, zinc-blende and rock-salt. At ambient conditions the wurtzite structure is the thermodynamically stable phase, consisting of two interpenetrating hexagonal close-packet lattices, which are shifted with respect to each other ideally by $3/8 \cdot c_0$, where $c_0$ is the height of the hexagonal lattice cell as shown in Fig. 2.1.[5] Each atom is tetrahedrally bonded to four atoms of the other type and the chemical bonds are

ionic due to the large difference in electronegativity of Ga and N atoms. Moreover, GaN is non-centrosymmetric along the [0001] direction or c-axis, which, by convention, is the direction of a vector pointing from a Ga atom to the nearest neighbor N atom. The lack of inversion symmetry means that, when defining an atom position on a closed-packed plane with coordinates (x, y, z,) it is not invariant to the position (-x, -y, -z) since the inversion results in the replacement of group III atoms by nitrogen atoms and vice versa. Consequently, all atoms in the plane at each side of a bond are the same. Hence, the wurtzite GaN crystal has two distinct faces, commonly known as Ga-face and N-face, which correspond to (0001) and $(000\bar{1})$ crystalline faces. Figure 2.1 shows the atomic arrangement in Ga-face GaN crystals. The occurrence of Ga or N-face depends on the growth conditions. These different polarities have different properties that affect both device technology and performance.[6] N-face crystals are chemically active which enables wet-chemical etching of the material, they suffer from a very rough surface morphology and high background doping concentration. Ga-face crystals have much smoother surface morphology and lower background doping concentration, which is beneficial for buffer resistivity and electrical device isolation. The disadvantage is that this material is almost chemically inert. Consequently, it can only be etched using plasma etching technique. Despite this difficulty, Ga-face crystals have superior electron transport properties and are preferred for device work.[7]

The work described in this thesis is based on Ga-face AlGaN/GaN HEMTs grown by metal organic chemical vapor deposition (MOCVD). We will shortly discuss the MOCVD technique in Chapter 4.

### 2.2.2 Spontaneous polarization

III-nitride compounds have a unique property due to the nitrogen, which is the smallest and most electronegative element in the group V. As mentioned in the previous section, the wurtzite III-nitride does not have inversion symmetry along the [0001] direction. This fact, in combination with the strong ionicity of nitrogen, results in a strong macroscopic polarization along the [0001] direction: the crystal is "naturally" distorted. Since this polarization effect occurs in the equilibrium lattice of III-nitrides at zero strain it is called spontaneous polarization ($P_{sp}$).[8] The electric field and charge sheet present in a Ga-face crystal of GaN and AlGaN grown on a c-plane due to the

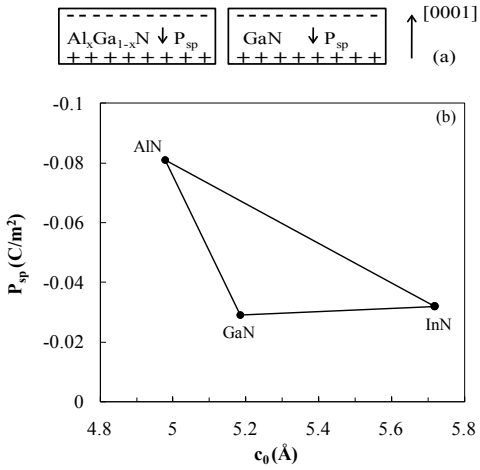


**Fig. 2.2** Electric field and charge sheet due to the spontaneous polarization in AlGaN and GaN crystals grown on a c-plane in a Ga-face crystal (a). Spontaneous polarization coefficients in AlN, GaN and InN system as a function of $c_0$ (b).[8]

spontaneous polarization is shown in Fig. 2.2a. The values of the spontaneous polarization coefficients in the GaN material system are shown in Fig. 2.2b.[8]

### 2.2.3 Piezoelectric polarization

If the ideality of the III-nitrides lattices is changed externally there will be changes in the polarization of the crystal. One way to change the ideality of the crystal lattice is through strain. This additional polarization is called strain-induced or piezoelectric polarization ($P_{pe}$).[8] In the AlGaN/GaN HEMT, due to the differences in lattice constant of AlN and GaN, the AlGaN layer on top of GaN, is grown with a tensile strain as shown in Fig. 2.3. The strength of the piezoelectric polarization can be calculated with the piezoelectric coefficients $e_{31}$ and $e_{33}$ as:

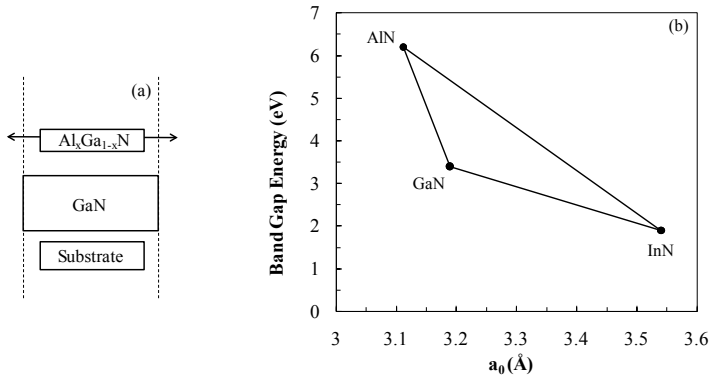


**Fig. 2.3** Strain in an AlGaN/GaN structure (a). Band gap energy as a function of the lattice constant (b).

$$P_{pe} = e_{33} \cdot \varepsilon_z + e_{31} \cdot (\varepsilon_x + \varepsilon_y) \tag{2.1}$$

where $\varepsilon_z = (c - c_0)/c_0$ is the strain along the c-axis, and the in-plane strain $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$ is assumed to be isotropic, with $a_0$ and $c_0$ being the equilibrium lattice constants. The different strains in the lattice are related as:

$$\varepsilon_z = -2 \cdot \frac{C_{13}}{C_{33}} \cdot \varepsilon_x \tag{2.2}$$

where $C_{13}$ and $C_{33}$ are elastic constants.

Equations (2.1) and (2.2) can be combined to obtain the following equation:

$$P_{pe} = 2 \cdot \frac{a - a_0}{a_0} \cdot \left[ e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right] \tag{2.3}$$

**Table 2.2** Constants used to calculate the polarization in III-nitride layers.[9]

| Constants | AlN | GaN | InN |
|---|---|---|---|
| $P_{sp}$ (C/m$^2$) | -0.081 | -0.029 | -0.032 |
| $e_{33}$ (C/m$^2$) | 1.46 | 0.73 | 0.97 |
| $e_{31}$ (C/m$^2$) | -0.6 | -0.49 | -0.57 |
| $C_{13}$(GPa) | 108 | 103 | 92 |
| $C_{33}$(GPa) | 373 | 405 | 224 |
| $a_0$ (Å) | 3.112 | 3.189 | 3.540 |

Since in the wurtzite III-nitrides the piezoelectric coefficient $e_{31}$ is always negative while $e_{33}$, $C_{13}$ and $C_{33}$ are always positive, it turns out that the term between brackets will always be negative. Consequently, the value of piezoelectric polarization in III-nitrides is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). As the spontaneous polarization in III-nitrides is always negative, it can be concluded that for layers under tensile stress spontaneous and piezoelectric polarizations are parallel to each other and with the same direction, while for layers under compressive stress they are appositively oriented. Table 2.2 shows the values of the constants used in the calculation of the polarization.[9] For $Al_xGa_{1-x}N$ we use the following set of linear interpolations between the physical properties of GaN and AlN[6]:

lattice constants:

$$a_0(x) = (-0.077x + 3.189) \cdot 10^{-10} \text{ m}, \tag{2.4}$$

elastic constants:

$$C_{13} = (5x + 103)\ \text{GPa}, \tag{2.5}$$

$$C_{33} = (-32x + 405)\ \text{GPa}, \tag{2.6}$$

piezoelectric constants:

$$e_{31}(x) = (-0.11x - 0.49)\ \text{C/m}^2, \tag{2.7}$$

$$e_{33}(x) = (0.73x + 0.73)\ \text{C/m}^2, \tag{2.8}$$

spontaneous polarization:

$$P_{sp} = (-0.052x - 0.029)\ \text{C/m}^2. \tag{2.9}$$

Since the lattice constant decreases with the increase of the Al content (Eq. 2.4) the AlGaN piezoelectric polarization increases with the Al content. Fig. 2.4 shows a cross-section of an AlGaN/GaN HEMT structure with the AlGaN layer under tensile strain and the calculation of the total polarization in the AlGaN layer. Both spontaneous and piezoelectric polarizations are parallel with the same direction and according to the previous equations they increase with the Al content. In general, if the polarization changes in space, there will be a charge density given by $\rho_P = -\nabla P$. At an abrupt interface of a top/bottom (AlGaN/GaN) heterostructure the polarization causes a polarization sheet charge density defined by

$$\sigma_{pol} = P(\text{bottom}) - P(\text{top}) = \{P_{sp}(\text{bottom}) + P_{pe}(\text{bottom})\} - \{P_{sp}(\text{top}) + P_{pe}(\text{top})\} \tag{2.10}$$

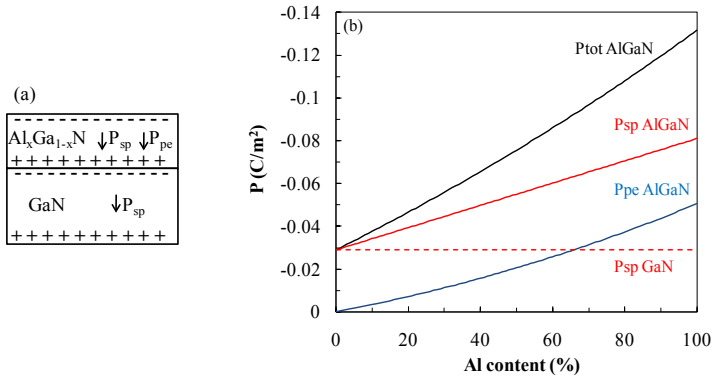


**Fig. 2.4** Combined piezoelectric and spontaneous polarization dipole in an AlGaN/GaN structure grown on c-plane in a Ga-face crystal (a). Calculation of the total polarization in the AlGaN crystal as a function of the Al content (b).

Since the GaN buffer layer is totally relaxed the GaN piezoelectric polarization is zero. Eq. (2.10) becomes:

$$\sigma_{pol} = P_{sp}(GaN) - \{P_{sp}(AlGaN) + P_{pe}(AlGaN)\} \tag{2.11}$$

Based on the values reported in Table 2.2 and on the equations reported above, the polarization induced sheet charge density is positive ($+\sigma$) as shown in Fig. 2.5. By increasing the Al content both piezoelectric and spontaneous polarizations of the AlGaN layer increase and consequently the sheet charge density increases.

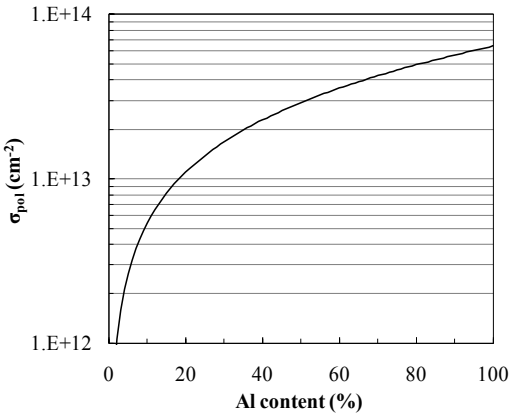


**Fig. 2.5** Polarization induced sheet charge density at the AlGaN/GaN heterointerface as a function of the Al content.

### 2.2.4 Formation of the 2DEG

If the polarization induced sheet charge density is positive ($+\sigma$), free electrons will tend to compensate the positive polarization induced charge at the AlGaN/GaN interface. These electrons will form a two dimensional electron gas (2DEG) with a sheet carrier concentration $n_s$, if the energy level in the quantum well at the AlGaN/GaN interface drops below the Fermi level, if the AlGaN/GaN band offset is reasonably high and if the interface roughness is low[7]. To keep the charge neutrality across the AlGaN barrier the net charge at the surface must be positive and therefore a positive compensating charge ($+\sigma_{surf}$) is required (Fig. 2.6). Consequently, any surface charge modification directly affects $n_s$. The origin of the 2DEG at the AlGaN/GaN heterointerface has been a topic for debate as the layers are not doped. According to Ibbetson *et al.*[11], the source of the electrons in the 2DEG is donor-like surface states which ionize only when the barrier thickness exceed a critical thickness $t_{CR}$. For a thin AlGaN barrier layer the surface state is at energy $E_D$ below the conduction band edge. This state is donor-like in the sense that it is neutral when occupied and positive when emptied. If this state is sufficiently deep it lies below the Fermi level (Fig. 2.7a) and there is no 2DEG. When increasing the barrier thickness $E_D - E_F$ decreases. At a certain

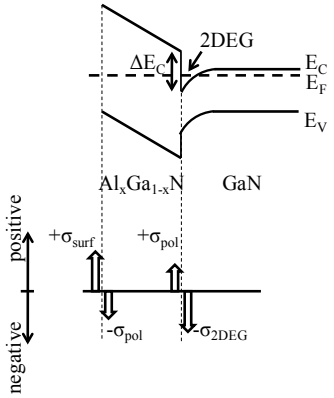


**Fig. 2.6** Band diagram of the AlGaN/GaN heterostructure with the formation of the quantum well and schematic of the charge densities at the heterointerface and at the AlGaN surface.

thickness, named critical thickness $t_{CR}$, the donor level reaches the Fermi level and electrons are able to transfer from occupied surface states to empty conduction band states at the interface creating the 2DEG and leaving behind positive surface charge (Fig. 2.7b). More and more electrons transfer when increasing the AlGaN barrier thickness approaching the polarization induced charge for $t \gg t_{CR}$ (Fig. 2.7c). The critical thickness $t_{CR}$ can be expressed as followed:

$$t_{CR} = (E_D - \Delta E_C) \cdot \frac{\varepsilon}{q\sigma_{pol}}, \tag{2.12}$$

where:

ε is the AlGaN dielectric constant:

$$\varepsilon(x) = -0.5x + 9.5, \tag{2.13}$$

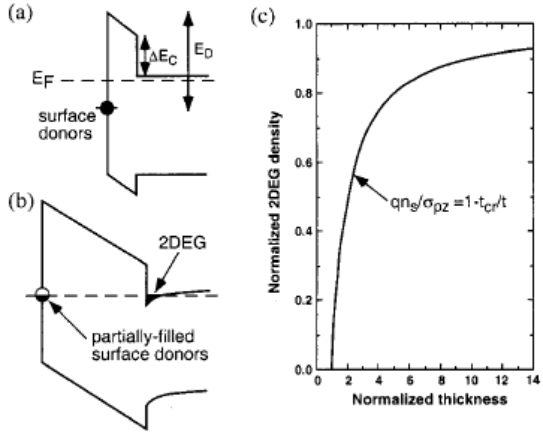


**Fig. 2.7** Schematic band diagram illustrating the surface donor model with the undoped AlGaN barrier thickness less than (a) and greater than (b) the minimum critical thickness for the formation of the 2DEG. Calculated 2DEG density as a function of the barrier thickness according to the surface donor model (c).[11]

$\Delta E_C$ is the conduction band offset:

$$\Delta E_C = 0.7\big(E_g(x) - E_g(0)\big)\ \text{eV}, \tag{2.14}$$

$E_{G\_AlGaN}$ is the AlGaN bandgap energy:

$$E_{G\_AlGaN}(x) = xE_G(\text{AlN}) + (1-x)E_G(\text{GaN}) - x(1-x)1.0\ \text{eV}, \tag{2.15}$$

and $E_D$ is the surface state energy. Figure 2.8a shows the critical thickness of the AlGaN barrier layer with surface states with energy $E_D$=$E_{G\_AlGaN}$/2 and without surface states. In this latter case, the only available occupied states are in the valence band. The 2DEG exists as long as the AlGaN barrier is thick enough to allow the valence band to reach

the Fermi level at the surface. Electrons can then transfer from the AlGaN valence band to the GaN conduction band, leaving behind a surface hole gas. The critical thickness is determined by the AlGaN band gap $E_{G\_AlGaN}$ instead of $E_D$ in Eq. (2.12).

For $t > t_{CR}$ the 2DEG density as a function of the barrier thickness is given by:

$$qn_s = \sigma_{PZ}\left(1 - \frac{t_{CR}}{t}\right) \tag{2.17}$$

where $\sigma_{PZ}$is the polarization induced charge. Figure 2.8b shows the 2DEG density in the case of surface states at energy $E_D$ and without surface states. Figure 2.9 shows the least-squares fit of the experimental values with $\sigma_{pz}$ and $t_{CR}$ as independent fitting parameters. The least-squares fit was achieved for $\sigma_{pz}$= $1.46 \cdot 10^{13}$ e/cm$^2$ and $t_{CR}$= 3.5 nm. Based on Eq. (2.12) they calculated the $E_D$ level at 1.65 eV below the AlGaN conduction band with a density as high as $1.1 \cdot 10^{13}$ cm$^{-2}$.[11] Koley and Spencer[12] measured a density of about $1.6 \cdot 10^{13}$ cm$^{-2}$ eV$^{-1}$ and an energy range of 1.0-1.8 eV

The nature of these surface donors has been discussed quite a lot. Jang[13] and Dong[14] concluded that these surface donors are oxygen impurities at 1.6 eV and 1.5 eV, respectively, from the conduction band due to the oxidation of the gallium terminated layer. Other research groups claimed that these surface donors are nitrogen vacancies ($V_N$).[15-18] During the high temperature annealing residual impurities can cause oxidation reaction at the AlGaN surface. Due to this reaction, the N atoms dissociate from Al-N and Ga-N bonds and could react with each other or with O atoms forming volatile molecules such as $N_2$ or $NO_x$[15]. By passivating the AlGaN surface with a SiN layer the 2DEG concentration increases due to the silicon acting as surface donating electrons.

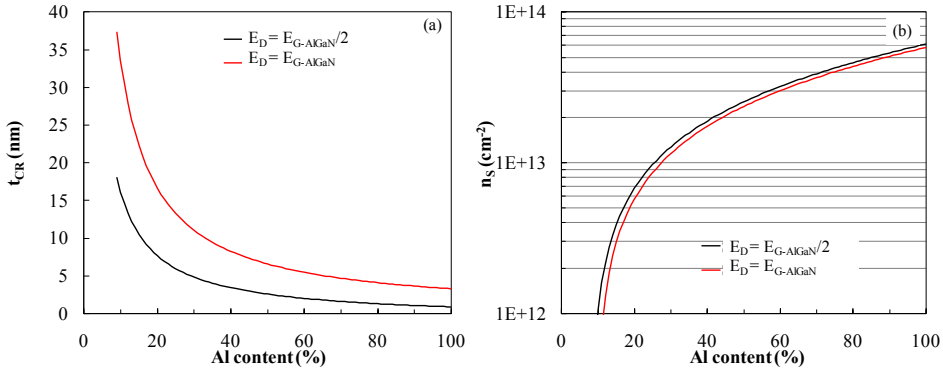


**Fig. 2.8** Theoretical critical thickness with surface states at energy $E_D = E_{G\_AlGaN}/2$ and without surface states $E_D = E_{G\_AlGaN}$ (a) and corresponding 2DEG density (b).

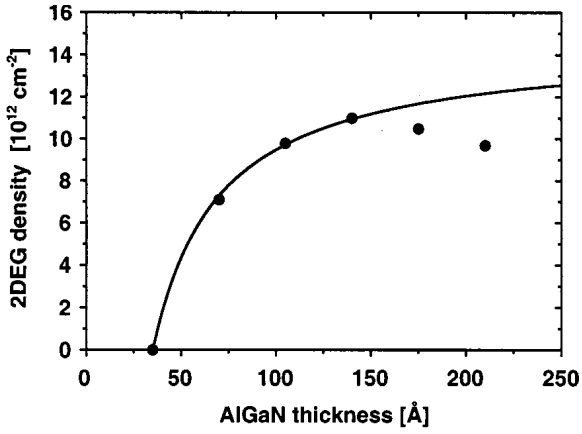


**Fig. 2.9** Room temperature 2DEG density measured as a function of $Al_{0.34}Ga_{0.66}N$ barrier thickness. The curve is the least-squares fit of Eq. (2.17) for the range $t < 15\ nm$.[11]

**Table 2.3** Sheet carrier concentration $n_S$, mobility μ and sheet resistance $R_S$ of the 2DEG of an AlGaN/GaN HEMT with and without the *in-situ* SiN passivation layer.

| | **2DEG w/o $Si_3N_4$** | **2DEG with $Si_3N_4$** |
|---|---|---|
| Sheet Carrier Conc. ($cm^{-2}$) | $1.1x10^{13}$ | $1.5x10^{13}$ |
| Mobility ($cm^2\ V^{-1}\ s^{-1}$) | 1200 | 1500 |
| Sheet Resistance (Ω/□) | 400 | 300 |

## 2.3 Imec *in-situ* SiN passivation

As we explained in the previous section, to keep the charge neutrality the 2DEG charge has to be equal to the AlGaN surface charge ($|\sigma_{2DEG}| = |\sigma_{surf}|$). The air exposure of the sample and any processing step can modify the AlGaN surface charge and, consequently, affect the 2DEG concentration. In order to protect this surface, Derluyn *et al.*[19] proposed the *in-situ* SiN passivation technique. It consists of the growth of a SiN layer directly in the MOCVD reactor without taking the sample out of the chamber. Si atoms passivate the nitride vacancies increasing the 2DEG. The most important feature is that a 2DEG channel is obtained even if the AlGaN barrier thickness is thinner than the critical thickness for which the 2DEG is not formed. This approach has been used in the realization of an enhancement-mode transistor which will be discussed in Chapter 6. In general, experimental data show (see Table 2.3) that the epilayer stack with the *in-situ* SiN layer has high mobility and low sheet resistance. Another advantage of this technique is that the SiN layer keeps the AlGaN barrier layer fully strained avoiding any strain relaxation, which would lead to lower $n_S$ values.[20]

## 2.4 Surface, bulk and interface defects in GaN

Due to the large lattice mismatch between GaN and Si several defects are expected during the growth, in particular edge and mixed type threading dislocations propagating from the bottom up to the surface. These dislocations, which can be electrical active, influence the buffer leakage current creating parasitic conducting paths which lower the breakdown voltage[21]. We will discuss this more in detail in Chapter 5 and 6.

Beside extended defects, our nitride epilayers show point defects such as impurities and vacancies. The main impurities are oxygen, silicon and carbon. Oxygen and silicon can be n-type dopants in GaN by substituting N ($O_N$) and Ga ($Si_{Ga}$) respectively. Oxygen contamination can come from the carrier gasses or precursors but also from the ambient during wafer loading and unloading. Silicon can come from the susceptor (SiC) but the concentration is lower than $10^{16}$ $cm^{-3}$. Carbon is a natural dopant in the MOCVD technique because it is contained in the precursors, like trimethylgallium ($Ga(CH)_3$) and trimethylaluminium ($Al_2(CH)_6$). It can be found as interstitial ($C_i$) as well as in substitutial position and its concentration depends on the growth conditions.[22] Under Ga-rich growth conditions carbon is a substitute for N ($C_N$) and is expected to be an acceptor in GaN. When the growth occurs under N-rich conditions carbon is a substitute for Ga ($C_{Ga}$) and is expected to be a donor.[23-24]. Fischer et al.[25] showed that $C_N$ is an acceptor in GaN with an optical binding energy of 230 meV. The introduction of the intentional Carbon doping is used to compensate the unintentional shallow donors present in the GaN layer, thereby rendering this layer more insulating.[22]

Others point defects in GaN are gallium vacancies ($V_{Ga}$) and nitrogen vacancies ($V_N$). $V_N$ are shallow donors. $V_{Ga}$ are deep acceptors and are found to be located at 3.26 eV below the conduction band.[17] These traps are reported to deteriorate device performance by causing current collapse.[26]

### 2.4.1 Current collapse phenomena

The current collapse, or also named dispersion, current compression, power slump etc.., is caused by deep traps in the material, especially by surface traps. It is

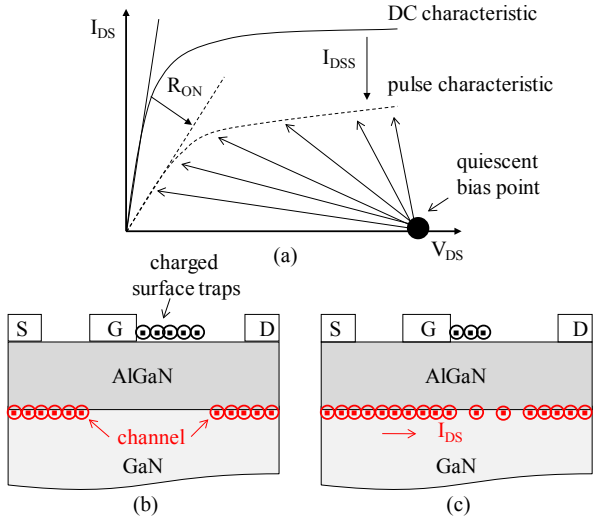


**Fig. 2.10** Schematic comparison of a DC I-V characteristic and a dynamic I-V characteristic when the device shows dispersion phenomena (a). Traps behavior in a device when it is turned-off (b) and turned-on (c).

measured as the discrepancy between the DC and pulse measurements. Pulse I-V measurement consists of applying a pulse signal that drives the device from a defined quiescent bias point (usually off-state at high drain bias) to points of the I-V plane in order to reconstruct the I-V characteristic as shown in Fig. 2.10a. When the device is turned-off, high electric field occurs at the gate edge on the drain side which can inject electrons into surface states between gate and drain. Consequently, the channel is depleted by the trapped electrons (Fig. 2.10b). When the device is turned-on, those trapped electrons should emit from the traps and let current pass through the channel (Fig. 2.10c). If the traps are deep, the emission process is considerably slow, resulting in slow channel current recovery (or slow switching speed) and consequently higher on-resistance ($R_{ON}$) and low saturated drain-source current ($I_{DSS}$). The capture of electrons injected from the gate during turn-off helps to increase the breakdown voltage. Indeed, as the trapping phenomena proceeds, the depletion region vertically extends mitigating the electric field at the gate edge on the drain site and, as consequence, the

breakdown voltage increases. But the electrons emit from these deep traps are too slow during turn-on, thus slow down the switching speed. Shallow surface traps can capture electrons during turn-off and emit them promptly during turn-on. This is desirable to obtain high breakdown voltage while maintaining fast switching speed.[27,28] It was demonstrated that the SiN passivation layer on top of the AlGaN layer causes Si to be incorporated as a shallow donor at the AlGaN surface in sufficiently large quantities to replace the surface states.[28,29] Therefore, as we stated previously, depositing a SiN layer *in-situ* directly in the MOCVD chamber increases the 2DEG and also reduces the dispersion phenomena. Moreover, an optimized surface field plate structure is effective for the suppression of the current collapse phenomena due to the relaxation of the electric field peak at the gate edge.[30] Moreover, it is worth to mention that these trapping phenomena can also occur in the GaN buffer layer due to deep traps close to the valence band and located far from the 2DEG. The time constants associated with this trapping process are very long in the order of minutes and hours. Therefore, they can also affect the device performance.[31] However, the recent and continuous improvement of the quality of the epilayer structure has lead to low bulk defects density. Consequently, the dispersion due to these traps is negligible.[32]

## 2.5 References


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# Chapter 3

# Simulations of AlGaN/GaN HEMTs

This chapter discusses two dimensional simulations of AlGaN/GaN HEMTs performed with Sentaurus Device simulator[1]. This tool is an advanced multidimensional device simulator capable of simulating electrical, thermal, and optical characteristics of silicon- and compound semiconductor-based devices. Simulations are very important because they provide key insights into device operation. The goal of our simulations is the qualitative analysis of band diagram, electric field at the AlGaN surface, impact of field plate and breakdown voltage. We will first discuss the models and the material parameters used in the simulations. Both SHFET and DHFET are simulated. In particular, we optimized the structure of the DHFET in terms of Al content and GaN channel thickness. High voltage simulations were performed to understand the breakdown mechanisms. We also demonstrate that the field plate technique is an effective way to reduce the surface and channel electric field in order to increase the breakdown voltage.

**Table 3.1** Material parameters at 300 K used in the simulations of AlGaN/GaN HEMTs[1].

| Material properties | AlN | GaN |
|---|---|---|
| Relative permittivity | 8.5 | 9.0 |
| Energy gap (eV) | 6.2 | 3.4 |
| Electron affinity (eV) | 1.9 | 3.4 |
| Electron mobility ($cm^2\ V^{-1}\ s^{-1}$) | 300 | 900 |
| Electron saturation velocity ($cm\ s^{-1}$) | $1.5 \times 10^7$ | $2.5 \times 10^7$ |
| Effective conduction band density of states ($cm^{-3}$) | $4.1 \times 10^{18}$ | $2.65 \times 10^{18}$ |

## 3.1 Material parameters and models

Since GaN is not a mature electronic semiconductor material, it is possible to find some discrepancies between theoretically calculated material parameters and those that are experimentally measured. The main material parameters for GaN and AlN used in the current simulations are listed in Table 3.1. The material parameters for the AlGaN layer are calculated by linear interpolation of GaN and AlN values. The charge at the heterointerface due to spontaneous and piezoelectric polarizations is calculated on the basis of the work of Ambacher *et al.*[2] The AlGaN barrier layer is totally strained and the GaN buffer layer relaxed. The density-gradient model (DG) is used in order to take the quantum effects into account.

### 3.1.1 Transport model

Depending on the device under investigation and the level of accuracy required, the user can select four different simulation transport models: drift diffusion, thermodynamic, hydrodynamic or Monte Carlo. The three governing equations for charge transport in semiconductor devices are the Poisson equation and the electron and hole continuity equations. The Poisson equation is:

$$\nabla \cdot \varepsilon \nabla \varphi = -q(p - n + N_D - N_A) - \rho_{trap}, \tag{3.1}$$

where $\varphi$ is the potential, $\varepsilon$ the electrical permittivity, q the elementary charge, n and p the electron and hole concentrations, $N_D$ is the concentration of ionized donors, $N_A$ the concentration of ionized acceptors and $\rho_{trap}$ is the charge density contribution by traps and fixed charges. The continuity equations for electrons and holes are:

$$\nabla \cdot \overrightarrow{J_n} = qR_{net} + q\frac{\partial n}{\partial t}, \qquad -\nabla \cdot \overrightarrow{J_p} = qR_{net} + q\frac{\partial p}{\partial t}, \tag{3.2}$$

where $R_{net}$ is the net electron-hole recombination rate, $\overrightarrow{J_n}$ is the electron current density and $\overrightarrow{J_p}$ is the hole current density. Depending on the transport model used in the simulation, the current density expressions are different. In our simulations we use the drift diffusion (DD) model or the hydrodynamic (HD) model. DD model assumes that the carriers are in thermal equilibrium with the lattice. HD model assumes that the electron and hole temperatures are not equal to the lattice temperature. Thus, the HD current density expressions are more complicated compared to the ones of the DD model because they take into account the carrier temperature gradients.

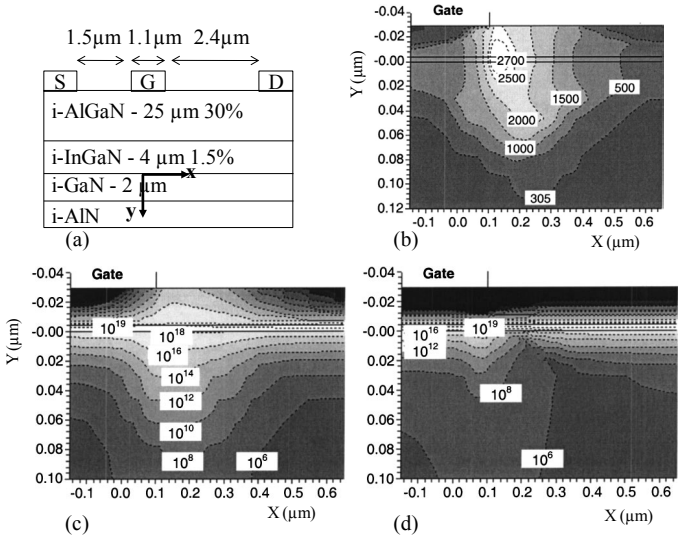


**Fig. 3.1** The SHFET used in the simulations (a). Cross-section of the SHFET around the gate edge at the drain side showing the electron temperature (K) (b) and the electron density ($cm^{-3}$) predicted by hydrodynamic (c) and drift diffusion (d) simulations for a bias of $V_{DS}$=10 V and $V_{GS}$= 0 V.[3]

To accurately simulate AlGaN/GaN heterostructures the HD model is needed because it takes into account the hot-electron effects. According to the work of Braga *et al.*[3], the HD model takes into account the capture of hot electrons at bulk traps under sufficient high drain bias conditions as shown in Fig. 3.1. The electron temperature distribution shows a hot spot in and around the channel near the gate edge at the drain side (Fig. 3.1b). The electrons in this location have enough energy to spread over the AlGaN barrier and towards the GaN bulk. Indeed, in DD simulations the electrons tend to be confined in the channel while in HD simulations the spreading of hot electrons towards the AlGaN barrier and the GaN buffer layer is evident. At higher drain bias, the electrons become hotter and thus, the spreading wider. Consequently, more trap levels inthe GaN buffer will be occupied with electrons. Hot electron spreading strongly affects the breakdown voltage and in the transient regime it may become the main contributor to the current collapse phenomenon. Faraclas *et al.* also point the attention on the use of

HD model together with the DG model in order to accurately simulate DC characteristics and quantum well effects of AlGaN/GaN devices.[4]

However, only in the simulations at high voltage we had to use the DD model in order to avoid convergence problem. Since the goal of our high voltage simulations is the qualitative study of the breakdown voltage, the use of the DD model is a good approximation. However, we will discuss the difference between DD and HD model in the high voltage simulations section.

### 3.1.2 Mobility model

Since in high electric fields, the carrier drift velocity is no longer proportional to the electric field but saturates to a finite speed $v_{sat}$ we used the Canali model:

$$\mu = \frac{(\alpha+1)\mu_{low}}{\alpha+\left[1+\left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}, \tag{3.3}$$

where $\mu_{low}$ is the low field mobility, $v_{sat}$ is the saturation velocity and $F_{hfs}$ is the driving force which depends on the transport model and $\alpha$ is a fitting parameter. We also included the mobility degradation due to impurity scattering. The exponent $\beta$ is temperature dependent according to:

$$\beta = \beta_0 \left(\frac{T}{300}\right)^{\beta_{exp}}, \tag{3.4}$$

$\beta$ and $\beta_{exp}$ are adimensional fitting parameters. We also used the high-field saturation model with temperature dependence if the HD model is switched on.

### 3.1.3 Avalanche model

Electron-hole pair production due to avalanche generation (impact ionization) requires a certain threshold field strength and the possibility of acceleration, that is, wide space charge regions. If the width of a space charge region is greater than the mean free path between two ionizing impacts, charge multiplication occurs, which can cause electrical breakdown. The reciprocal of the mean free path is called the ionization coefficient α. With these coefficients for electrons and holes, $\alpha_n$ and $\alpha_p$, the generation rate can be expressed as:

$$G = \alpha_n n \nu_n + \alpha_p p \nu_p, \tag{3.5}$$

$\nu_n$ and $\nu_p$ are the electron and hole drift velocities. The avalanche model used in our high-voltage simulation for the DD transport model is the Van Overstraeten-de Man model, where the ionization coefficient is given by:

$$\alpha = \alpha_0 \cdot e^{-b/E}, \tag{3.6}$$

where E is the electric field intensity, $\alpha_0 = 2.9 \cdot 10^8$ cm$^{-1}$ and $b = 3.4 \cdot 10^7$ V/cm for GaN[5].

With the HD transport model the temperature dependence has to be included. The high voltage simulations with the HD transport model show convergence problem especially when the device is simulated in a strong pinch-off condition. Since the scope of our simulation is the qualitative analysis of the breakdown voltage in different structures we used the DD transport model with the Van Overstraeten-de Man avalanche model. We will explain the impact of DD and HD models on high-voltage parameters in the next section.

### 3.1.4 Trap model

Sentaurus Device provides several trap types combined with different types of energetic distribution and various models for capture and emission rates. These traps are available for both bulk semiconductors and interfaces. As we mentioned in Chapter 2, the GaN epi-materials have a significant amount of defects such as dislocations and impurities which translate into traps. In order to take these traps into account we introduce acceptor single level traps in the AlGaN and GaN layer. They are uncharged when unoccupied and they carry the charge of one electron when fully occupied. The density of acceptor type traps is $5 \cdot 10^{17}$ $cm^{-3}$ with a cross section of $1 \cdot 10^{-15}$ $cm^{-2}$ positioned at 1 eV above mid band gap. The Shockley-Read-Hall model is used to take the recombination through deep defect levels in the gap into account. However, for III-nitride materials the trap parameters are still largely unknown.

## 3.2 Simulation of AlGaN/GaN SHFET

The first step of a simulation is the creation of a device structure in Sentaurus Device editor module to model the device geometry and create a mesh of nodes where the solutions to the basic equations would be computed. Next, the material parameters are entered. Last, the electrode and the physics are entered. The simulated AlGaN/GaN SHFET is shown in Fig. 3.2. The source and drain ohmic contacts are simulated as highly doped regions. The length of each ohmic contact is 1 µm. In the experimental work we use Ni/Au metal for the Schottky gate so the barrier height was set to 1.25 eV. Both AlGaN and GaN layers are undoped and the thickness of the SiN passivation layer is 150 nm. The source-gate ($L_{SG}$) spacing and gate length ($L_G$) are 1.5 µm and the gate-drain distance ($L_{GD}$) is 2 µm. We first simulate the transistor characteristics. Figure 3.3a shows simulations of $I_{DS}$-$V_{DS}$ curves for -3 V < $V_{GS}$ < +1 V with a step of 1 V and Fig.3.3b shows the $I_{DS}$-$V_{DS}$ measurements performed on a device with gate-drain distance of 5 µm for -4 V < $V_{GS}$ < +2 V with a step of 2 V. This comparison shows that our simulations are in good agreement with our measurements. Indeed, the simulated saturation current is in the same range as the measured saturation current. The slope of the $I_{DS}$ curves is slightly different due to the not optimized ohmic contacts in the simulations and also due to the different $L_{GD}$. Fig. 3.4 shows the simulated $I_{DS}$-$V_{GS}$ curve for $V_{DS}$= 10 V. Figure 3.5 shows the conduction band profile and electron density

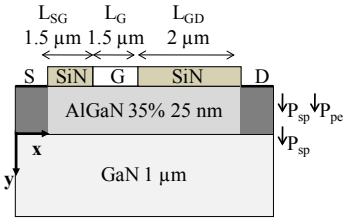


**Fig. 3.2** AlGaN/GaN SHFET used in the simulations.

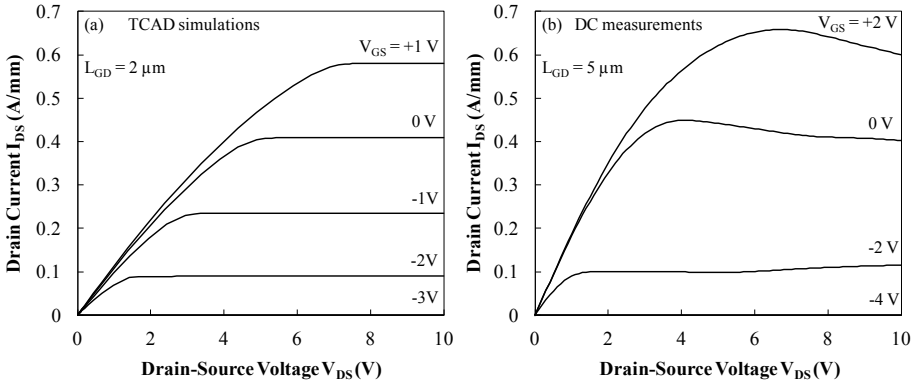


**Fig. 3.3** Simulations of $I_{DS}$-$V_{DS}$ curves of AlGaN/GaN SHFET with $L_{GD}$ = 2 µm (a). DC measurements of a device with $L_{GD}$ = 5 µm (b).

extrapolated at the gate edge at the drain side. As we explained in Chapter 2, electrons fill the quantum well at the heterointerface due to the difference in polarization between AlGaN and GaN. As expected for depletion-mode devices, the electron density in the channel decreases with increasing of the negative gate bias. Figure 3.6 shows the electron density in the channel for $V_{GS}$= 0 V and $V_{GS}$= -6 V and a drain bias of $V_{DS}$= 10 V. The values are extrapolated at the gate edge at the drain side (X= 4 µm). At $V_{GS}$= -6 V the device is in pinch-off condition. Thus, the channel under the gate is depleted.

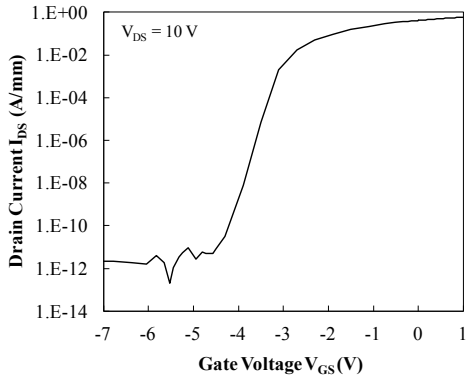


**Fig. 3.4** Simulated $I_{DS}$-$V_{GS}$ characteristic with $V_{DS}$ = 10 V of AlGaN/GaN SHFET with $L_{GD}$ = 2 μm.

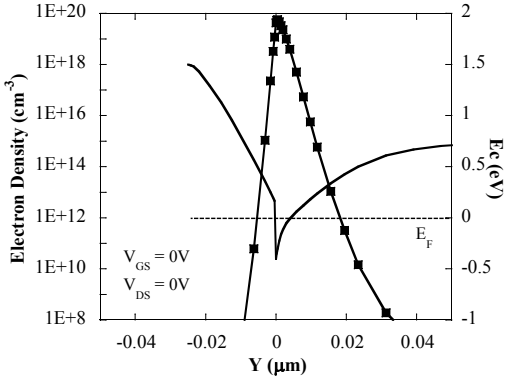


**Fig. 3.5** Depth electron density and conduction band profiles at thermal equilibrium $V_{GS}$ = 0 V and $V_{DS}$ = 0 V. Y = 0 μm is the AlGaN/GaN heterointerface.

The main issue of this device is the strong electric field at the gate edge at the drain side which is the sum of a vertical and a horizontal electric field. Since the surface traps are the source of the 2-DEG, when they are filled with the electrons injected from the gate the channel is vertically depleted to keep the system electrically neutral. In the

lateral direction, the drain bias generates a constant electric field $E_x$ in the neutral region. The polarization field $E_p$ is very strong in AlGaN and is as high as several MV/cm. Therefore, the total field in the depletion region is a combination of the lateral field $E_x = V_{GD}/d_1$ where $d_1$ is the depletion region length, and of the vertical field $E_p$: $E_{tot} = \sqrt{E_p^2 + E_x^2}$. Assuming that the gate-drain region is fully depleted when the device is biased to breakdown, the lateral electric field becomes $E_x \cong V_{BR}/L_{GD}$ and $E_{tot}$ is the critical electric field. Figure 3.7 shows the electric field distribution which peaks at the gate edge with the increase of the negative gate voltage. Figure 3.8 shows the electric field extrapolated at the AlGaN surface under different bias conditions. In pinch-off condition $V_{GS}$= -6 V, the electric field peaks to a value as high as 3.7 MV/cm for $V_{DS}$= 10V and increases with the increase of the drain bias. This high electric field causes the device breakdown. The field plate technique, presented later, helps in reducing this peak and consequently increases the breakdown voltage.

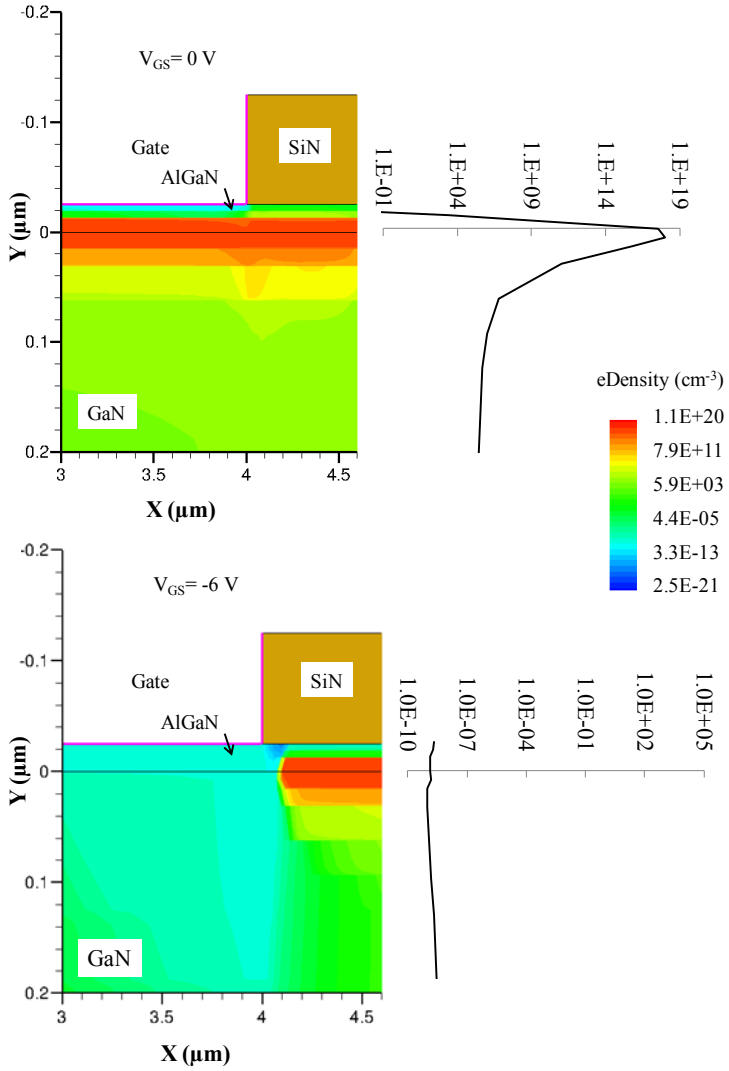


**Fig. 3.6** Electron density simulated at $V_{GS}$= 0 V and $V_{GS}$= -6 V for a drain bias of $V_{DS}$= 10 V. Y=0 µm is the AlGaN/GaN heterointerface.

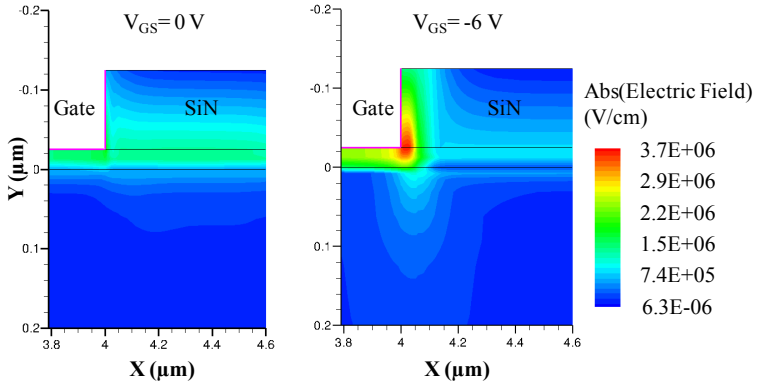


**Fig. 3.7** Electric field simulated at $V_{GS}$= 0 V and - 6 V for a drain bias of $V_{DS}$= 10 V. Y= 0 µm is the AlGaN/GaN heterointerface.

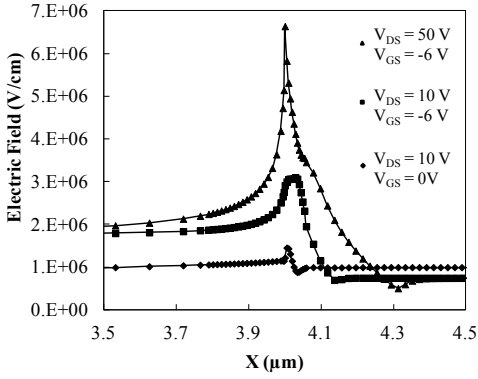


**Fig. 3.8** Electric field at the AlGaN surface under different bias conditions.

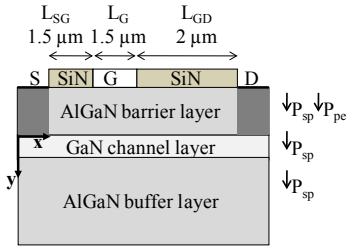


**Fig. 3.9** AlGaN/GaN/AlGaN double heterostructure (DHFET).

## 3.3 Simulation of AlGaN/GaN/AlGaN DHFET

According to the Baliga's figures of merit, discussed in Chapter 1, high mobility and high critical electric field are needed to minimize the conduction and switching losses in power switching applications. Also, in order to decrease the specific on-resistance the 2DEG carrier density has to be as high as possible. Thus, to improve device performance an increase of both 2DEG mobility and density is needed. This can be done taking advantage of the spontaneous and piezoelectric polarization effects. These effects largely influence the electrical properties in the heterostructure such as potential profile and electron density. A double heterostructure is formed by inserting a thin GaN layer grown in between two AlGaN layers, which we call the channel layer (Fig. 3.9). The top AlGaN layer is called barrier layer and the bottom one is called buffer layer. Like in our real epistructure, the AlGaN barrier layer is under tensile strain, the GaN channel layer and the AlGaN buffer layer are totally relaxed. Due to the polarizations a positive charge is present at the heterointerface between the AlGaN barrier layer and the GaN and a negative charge emerges at the second heterointerface between the GaN layer and the AlGaN buffer layer. In SHFET only a positive charge emerges at the AlGaN barrier layer and the GaN layer heterointerface. The most important feature of the DHFET is the enhancement of the 2DEG mobility and of the 2DEG electron distribution as Fig. 3.10 shows.

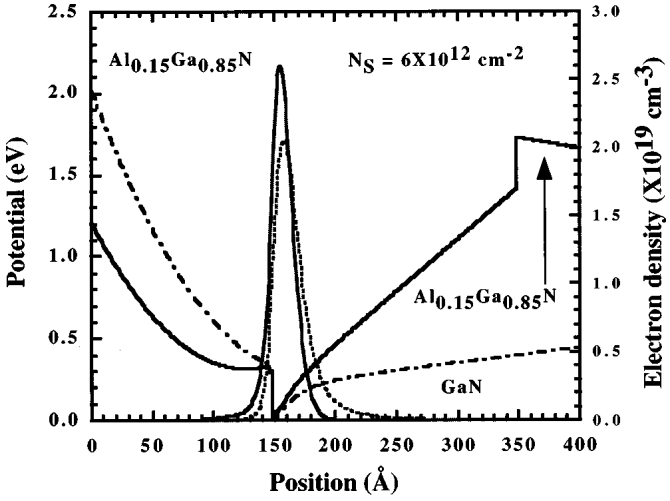


**Fig. 3.10** Dependency of 2DEG density in SH- and DH-FET.[6]

The enhancement in the mobility might be due to the enhancement of the screening effect and to the improvement in the interface roughness.[6] The electron distribution width of the 2DEG in DH is smaller than that in SH because the electrons in the GaN channel are repulsed by the negative polarization charge at the GaN/AlGaN buffer layer interface. Consequently, the electron density peak in DH becomes larger than that in SH as it is shown in Fig. 3.10. The enhancement in the electron confinement reduces the buffer leakage current and the use of the AlGaN as buffer layer increases the buffer critical electric field. These facts lead to the enhancement of the breakdown voltage as we will show in Chapter 5. For this reason we optimized the electrons confinement in DHFET structures in terms of GaN channel thickness and Al content of the AlGaN buffer layer with simulations.

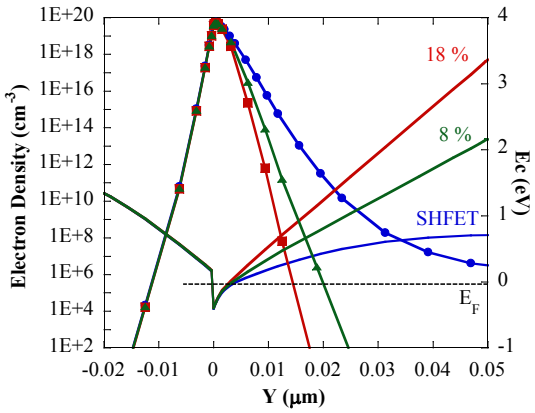


**Fig. 3.11** Conduction bands and electron densities of a SHFET (blue curves) and a DHFET with an AlGaN buffer layer with 8 % (green curves) and 18 % (red curves) of Al content. The simulations were done at thermal equilibrium.

### 3.3.1 Optimization of the Al content in the AlGaN buffer layer

As a first study, we simulated the impact of different Al content of the AlGaN buffer layer on the electron confinement. We used the DHFET structure shown in Fig. 3.9 with an AlGaN barrier thickness of 25 nm and an Al content of 35%. The GaN channel thickness is 50 nm and the AlGaN buffer layer is 1 µm thick. The DHFET was simulated for two different buffer Al contents: 8 % and 18 %. The negative charge increases with the Al content as the spontaneous polarizations of the AlGaN buffer layers increases with the Al content as shown in Chapter 2. The simulations were done at thermal equilibrium ($V_{GS}$=0 V and $V_{DS}$=0 V). Figure 3.11 shows the conduction band and the electron density profiles. The increase of the Al content in the buffer layer leads to higher conduction band profile. Consequently, a better electron confinement in the 2DEG is achieved and fewer electrons can spread into the buffer. However, the thickness of the GaN channel layer plays an important role in improving the electron confinement and increasing the electron density peak. We will show this in the next section.

### 3.3.2 Optimization of the GaN channel thickness

We simulated a DHFET structure with three different channel thicknesses: 50 nm, 100 nm and 150 nm. In these simulations the Al content of the AlGaN buffer layer was 18 %. Figure 3.12 shows the electron density distribution. Fig. 3.13 shows the electron density and the conduction band profile extrapolated at the gate edge. The electron density improves with the increase of the GaN channel layer thickness up to 150 nm.

The DHFET with a GaN channel thickness of 150 nm shows the highest electron density and the highest barrier among the three values simulated. The conduction band in the buffer is raised and fewer electrons can spread into the buffer layer. Consequently, the electron density peak is comparable with that one of the SHFET.

The electric field distribution is shown in Fig. 3.14. The DHFET with a GaN channel thickness of 150 nm confines the electric field in the channel and it is less spread into the buffer layer compared to the cases with 50 nm and 100 nm as channel thickness. The gate electric field peak, shown in Fig. 3.15, slightly increases with the GaN thickness. The value of the DHFET with 150 nm of the channel thickness is comparable with the electric field peak of the SHFET.

Based on these simulations, we decided to fabricate the DHFET structures with a channel thickness of 150 nm. Moreover, we also simulated this structure with different Al content of the AlGaN buffer layer. We used the Al content of 2 %, 4 %, 8 % and 18 %. These simulations show that, for a channel thickness of 150 nm, the electron density distribution saturates at 4 % as shown in Fig. 3.16. However, in the real structure we used Al content as high as 18 % because this AlGaN layer has higher band gap energy and critical electric field. Consequently, the buffer leakage current is reduced and higher buffer breakdown voltage can be reached. We will show this in Chapter 5. Finally, our optimized DHFET has a channel thickness of 150 nm and an AlGaN buffer layer with 18 % Al content. Fig. 3.17 summarizes the advantages of the DHFET over the SHFET showing a narrower electron density distribution due to the AlGaN buffer layer.

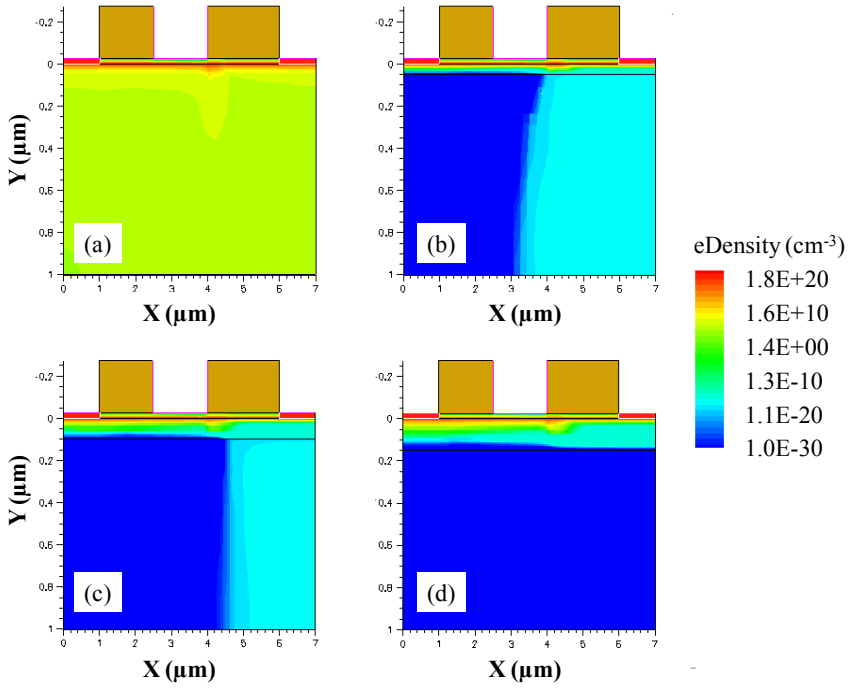


**Fig. 3.12** Electron density distribution in the SHFET (a), in the DHFET with a GaN channel thickness of 50 nm (b), 100 nm (c) and 150 nm (d). The simulations were done with $V_{GS}$= 0 V and $V_{DS}$ =10 V.

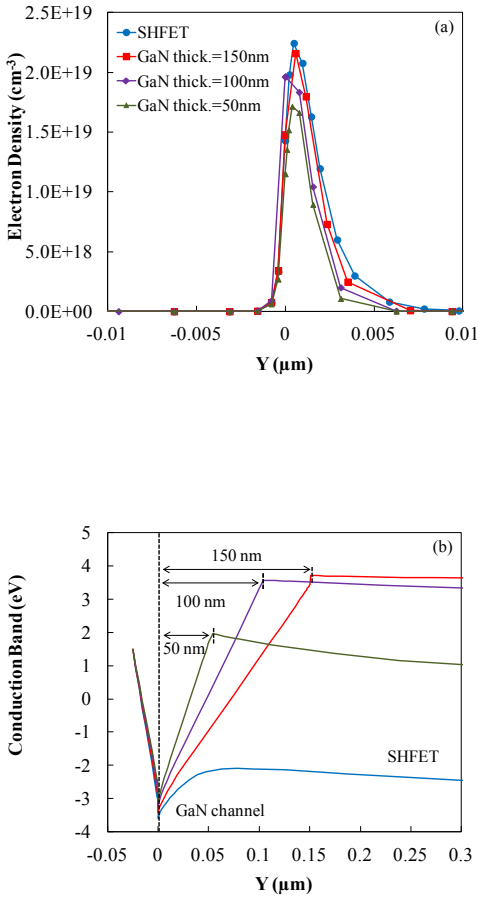


**Fig. 3.13** Depth electron density (a) and conduction band profiles (b) extrapolated at the gate edge (X = 4 µm). The electron confinement improves with the GaN thickness due to the higher conduction band of the 150 nm GaN channel thickness. The electron density peak for the GaN thickness of 150 nm (red curve) becomes comparable with the SHFET electron density peak (blue curve). Y = 0 µm is the heterointerface between the AlGaN barrier layer and the GaN layer.

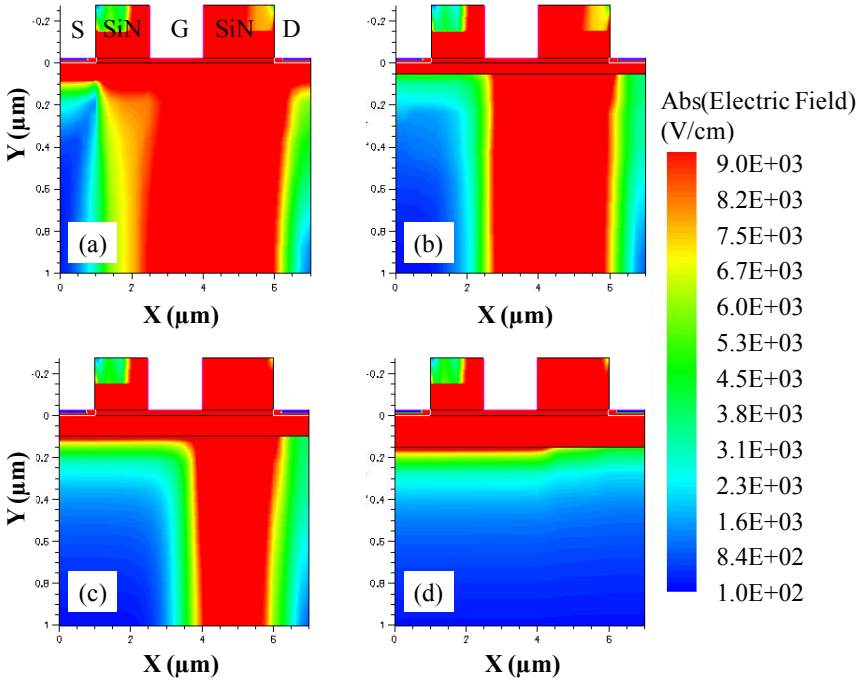


**Fig. 3.14** Electric field distribution in the SHFET (a), in the DHFET with a GaN channel thickness of 50 nm (b), 100 nm (c) and 150 nm (d). The simulations were done with $V_{GS}$= 0 V and $V_{DS}$ =10 V.

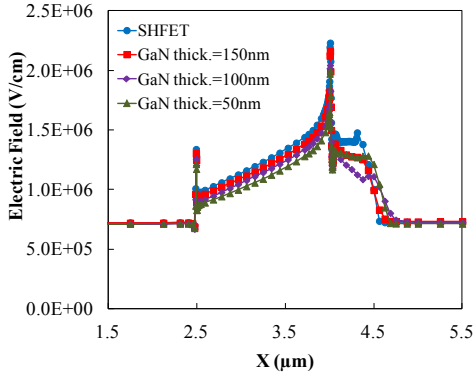


**Fig. 3.15** Electric field extrapolated at the AlGaN surface. The gate electric field slightly increases with the GaN channel thickness. The electric field peak of the DHFET with 150 nm of channel thickness (red curve) is comparable with the value of the SHFET (blue curve).

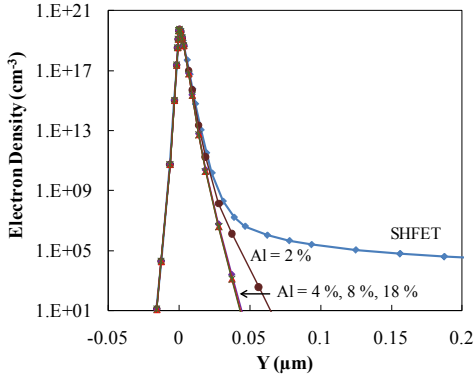


**Fig. 3.16** Depth electron density profile in SHFET and DHFET with the GaN channel thickness of 150 nm and 2 %, 4 %, 8 % and 18 % of Al content of the AlGaN buffer layer.

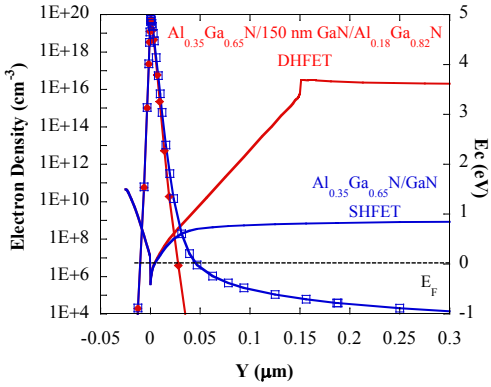


**Fig. 3.17** Depth profile of electron density and conduction band in SHFET (blue curve) and optimized DHFET (red curve). Simulations were done at thermal equilibrium.

## 3.4 High voltage characteristics

To simulate the breakdown characteristics we have to use the drift-diffusion (DD) transport model in order to avoid convergence problems. As we have shown in Fig. 3.1, with the DD transport model the electrons are confined in the channel and do not spread into the buffer. This is due to the fact that this model neglects the hot electron effects and assumes the same temperature for electrons, holes and lattice. Due to this fact the 2DEG channel at the breakdown value is not fully depleted. The reason is that the high electron temperature near the gate edge on the drain side leads to enhanced thermionic emission (TE) of the electrons from the channel into the AlGaN. The escape of electrons results in further depletion of the channel and considerable modification of the distributions of the carrier density, the electric field and electron temperature along the channel.[7,8] However, for a qualitative study of the breakdown voltage and of the field plate technique hot electron effects can be neglected and the drift-diffusion model can be used.

As we mentioned in the paragraph 3.2, when the channel is pinched-off and the drain is positive biased (OFF-state of a switching device) the electrons will inject into

the surface traps from the gate. Since the surface traps are the origin of the 2DEG, when they are filled with the injected electrons, the channel charge is vertically depleted to keep the system electrically neutral. By increasing the drain bias, more surface traps will be filled in and the channel depletion laterally extends. As we stated in the paragraph 3.2, the electric field peaks at the gate edge on the drain side and causes the breakdown of the device.

In the simulations the device is biased below pinch-off with $V_{GS}$= -8 V. The drain voltage is increased until the drain current rises sharply due to impact ionization. We define the breakdown voltage as the voltage where the impact ionization induced current rapidly rises. Fig 3.18 shows the breakdown characteristic of the SHFET device shown in Fig. 3.2 with $L_{GD}$= 2 μm. Figure 3.19 shows the electric field at the $Al_{0.35}Ga_{0.65}N$ surface at the breakdown conditions. The electric field peak is about 6.3 MV/cm which is assumed to be the critical electric field of the $Al_{0.35}Ga_{0.65}N$ surface layer. A qualitative correlation between simulations and experiments performed at high voltage was found and this will be discussed in Chapter 6.

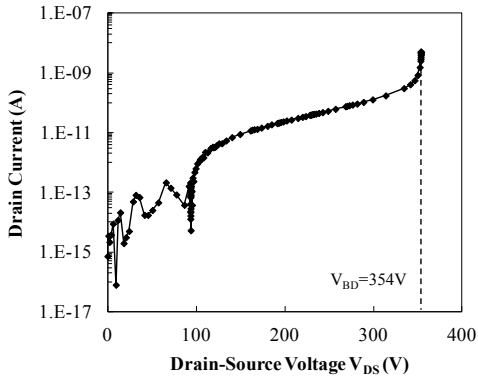


**Fig. 3.18** Breakdown characteristic of the SHFET with $L_{GD}$ = 2 μm.

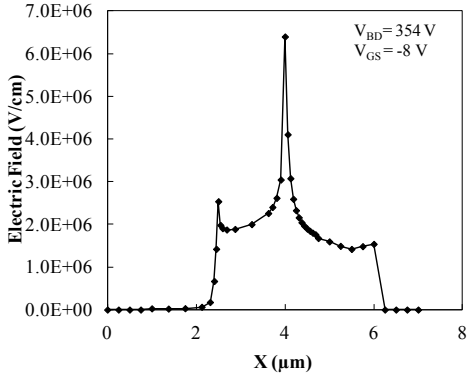


**Fig. 3.19** The electric field extrapolated at the gate edge at the drain side. The peak is around 6.3 MV/cm which is close to the critical electric field of $Al_{0.35}Ga_{0.65}N$ barrier layer.

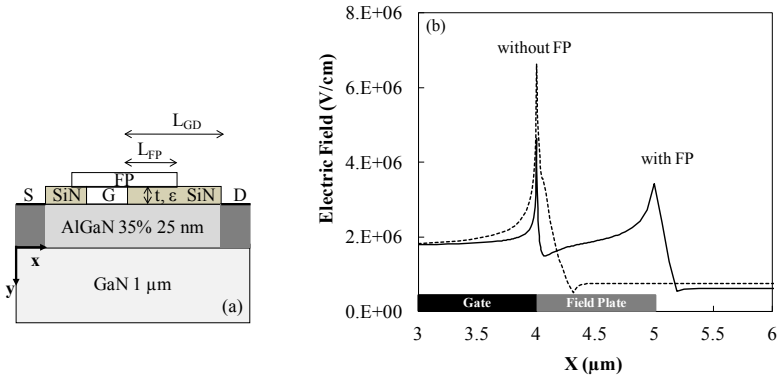


**Fig. 3.20** AlGaN/GaN SHFET with the field plate connected to the gate (a). Electric field at the gate edge on the drain site without and with field plate (b).

## 3.5 The field plate technique

As we showed above, in pinch-off condition the maximum electric field occurs at the gate edge at the drain side. Without passivation the surface states adjacent to the gate fill up with electrons thereby extending the depletion region width. This reduces the electric field peak that is seen at the gate edge thus enhancing the breakdown voltage. However, this causes dispersion as the surface states do not respond fast to the changes of the gate bias. The dispersion can be eliminated by passivating the surface with a SiN layer, as we discussed in the previous chapter. After passivation the electric field lines peak at the gate edge thereby reducing the breakdown voltage. A good trade-off between speed and breakdown voltage is needed. The best way to control the electric field without compromising the speed too much is the field plate (FP) technique[9]. Figure 3.20a shows the SHFET device with a gate connected field plate. A field plate is a metal electrode which offers an additional edge for the electrical field lines to terminate at higher drain bias. It extends the depletion region creating a second peak at the field plate edge and reducing the electric field peak at the gate edge as Fig. 3.20b shows. Thus, the breakdown voltage of the device increases. Also, since the field plate is a metal electrode, the response time is much faster than that of the surface states.[10] The field

plate can be electrically connected either to the source or to the gate. Since the gate-connected field plate offers a better reduction of the electric field peak compared to the source-connected field plate we fabricated our devices with a gate-connected field plate. For the optimization of the field plate geometry we followed the work of Karmalkar *et al.*[9,11] The critical variables associated with the FP are the three geometrical variables, namely FP length ($L_{FP}$), insulator thickness (t) and gate-drain distance ($L_{GD}$). In the HEMT without a FP, shown in Fig. 3.2, the breakdown field distribution at the AlGaN surface is confined over a small distance from the gate edge. Thus, a high field is reached even for small values of drain voltage as shown in Fig. 3.8. Consequently, the breakdown voltage ($V_{BD}$) is low. The FP reduces and spreads this field and consequently increases the breakdown voltage. The maximum $V_{BD}$ is obtained with an optimum t. This is because, for large t, the FP effect vanishes and the electric field distribution is concentrated at the gate edge. For t=0, the FP simply extends the gate by the FP length and the gate electric field peak is shifted at the FP edge. Thus $V_{BD}$ is low and equal of the one of a simple HEMT for the extreme cases of large t and t=0.

The optimum t increases with the increase of the insulator dielectric constant (ε) because the FP influences the electric field by capacitive action (roughly $t \propto \varepsilon$). The breakdown voltage $V_{BD}$ does not increase with the increase of $L_{FP}$ beyond a certain value because the overlap of the two peaks decreases with the increase of $L_{FP}$. $V_{BD}$ is the total area under these peaks for a given peak breakdown field; the increase in this area will saturate as the overlap of the two peaks decreases with the increase of $L_{FP}$. $V_{BD}$ won't increase with the increase of $L_{GD}$ beyond a certain point because the field distribution decays beyond the FP edge.

Based on these observations, we first optimized the passivation thickness t and afterwards the FP length ($L_{FP}$). The electric field at the surface is much higher than the one in the channel[11] .Therefore, we focus on the electric field peak at the surface. Fig. 3.21 shows the surface electric field with and without field plate. Three different passivation thicknesses are simulated: 50 nm, 100 nm and 200 nm. As we mentioned above, the field plate effect vanishes with increasing of the passivation thickness. Indeed, for t= 200 nm the field plate peak is rather low while the gate peak is the highest in both structures. In the DHFET, for t= 50 nm the field plate peak is higher compared to the gate peak, making the device break at the FP edge. For t= 100 nm the electric field is

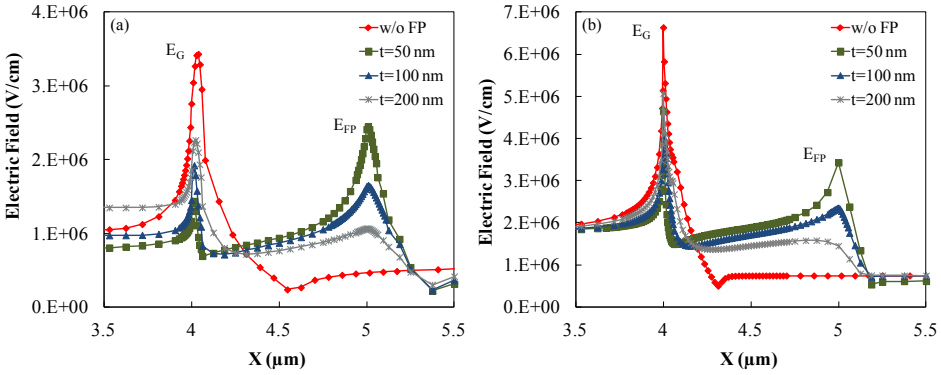


**Fig. 3.21** Electric field at the (a) AlGaN/GaN/AlGaN DHFET and (b) AlGaN/GaN SHFET surface. $E_G$ and $E_{FP}$ are the electric field peaks at the gate (X = 4 µm) and the FP (X = 5 µm) edge at the drain side, respectively. The field plate length is 1 µm and the gate-drain distance is 5 µm.

equally distributed between the two edges. Thus, in the DHFET, we decided to fix 100 nm as passivation thickness. In the SHFET, for t= 50 nm the two peaks are slightly different while for t= 100 nm the gate peak is higher than the FP peak. Thus, the optimum thickness for SHFET is a value between 50 nm and 100 nm. This is expected because the electric field peak without FP is higher in the SHFET than in the DHFET. Consequently, the SHFET needs a stronger FP action. Next, we simulated DHFET devices with different field plate lengths. This step is important because the gate capacitance increases with the field plate length thus a short FP length is needed. Fig. 3.22 shows that for $L_{FP}$= 1 µm the electric field is again equally distributed. For $L_{FP}$= 2 µm the electric field at the gate edge is increased. Thus, based on these simulations the optimum passivation thickness is 100 nm and the optimum field plate length is 1 µm.

We used nitride as passivation layer as it has higher dielectric constant (7.5) compared to, for example, oxide (3.9). The same simulations performed with the oxide as passivation layer show an optimum passivation thickness thinner than 50 nm.

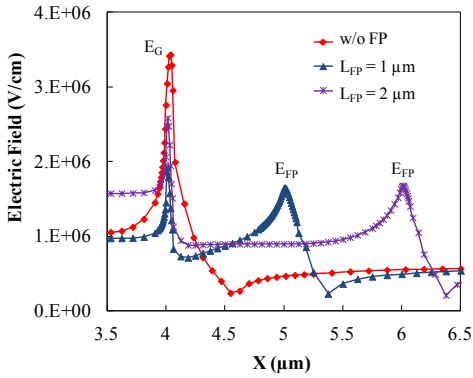


**Fig. 3.22** Electric field at the AlGaN/GaN/AlGaN DHFET surface with a field plate length of 1 µm and 2 µm. The passivation thickness is 100 nm.

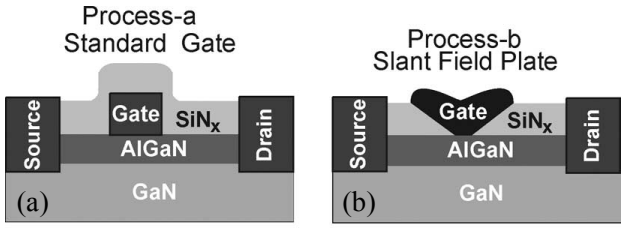


**Fig. 3.23** SHFET without field plate (a) and with slant field plate (b).[14]

Multiple (n) field plate can be used, each with increasing lateral extension from the gate and increasing vertical distance from the AlGaN surface. The single electric field peak is split in (n+1) smaller peaks[12,13]. An alternative to discrete multiple field plates is the "slant field plate" which offers a better reduction of the gate electric field peak over the single and multiple field plate technique. The field plate is integrated with the gate during the recess process of the gate in the same lithography step as Fig. 3.23 shows.[14] Simulations of different field plate designs were performed by Turin *et al.*[15] In Chapter 6 we will show the effect of the field plate on breakdown voltage and on-resistance.

## 3.6 References


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# Chapter 4

# Device Fabrication and Measurement Configurations

This chapter describes the fabrication of our GaN based devices and the measurement configurations for measuring the on-resistance and both buffer and device breakdown voltage in the horizontal and vertical direction. It starts with the description of the MOCVD growth of both SHFET and DHFET epilayer structures. In order to analyze the impact of the device geometry parameters on breakdown voltage we designed a dedicated mask. This mask, called “PowerSwitch”, uses test structures with different device geometries such as field plate length, gate-drain distances, gate lengths, gate widths and gate-source distances. Finally, we will describe the electrical configurations used for measuring the horizontal and vertical buffer and device breakdown voltage.

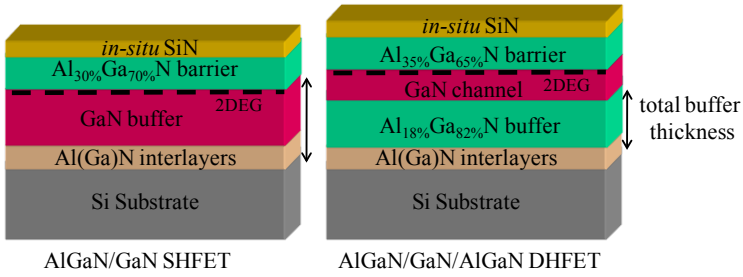


**Fig. 4.1** Layer structure of SHFET and DHFET used in our experiments.

## 4.1 MOCVD

The epitaxy of GaN-based heterostructures on 100 and 150 mm Si (111) substrates by Metal Organic Chemical Vapor Deposition (MOCVD) was carried out in a Thomas Swan CCS (close coupled showerhead) reactor[1,2]. We used highly resistive Float-Zone (FZ) 600 µm thick Si substrates with a resistivity as high as 5 kΩ·cm as well as highly doped 800 µm thick Czochralski (CZ) Si substrates with a resistivity as low as 0.1-100 Ω·cm. In Chapter 5 we will study the impact of the Si substrate doping on buffer breakdown voltage and buffer leakage current. Trimethylgallium ($Ga(CH_3)_3$), Trimethylaluminium ($Al_2(CH)_6$), Ammonia ($NH_3$) and Silane ($SiH_4$) are used as precursors for Ga, Al, N, and Si, respectively. Hydrogen ($H_2$) was used as carrier gas. Before starting the growth of the nitride layers, the silicon substrates were first annealed under hydrogen at 1120°C for 10 min. Figure 4.1 shows the layer structure for SHFET and DHFET. The epitaxial structure for both AlGaN/GaN SHFET and AlGaN/GaN/AlGaN DHFET starts with a 200 nm AlN nucleation layer. For the SHFET, the nucleation layer is followed by an $Al_{40\%}Ga_{60\%}N$ intermediate layer of 400 nm thickness and by a 1.3 µm thick GaN buffer layer. On top of this, 22 nm of $Al_{30\%}Ga_{70\%}N$ is grown as barrier layer followed by 3.5 nm of *in-situ* SiN as capping layer. For DHFET, the nucleation layer is followed by two or three AlGaN intermediate layers with 70 %, 40 % and 25 % Al content. On top of this 1 µm or 1.5 µm thick $Al_{18\%}Ga_{82\%}N$ is

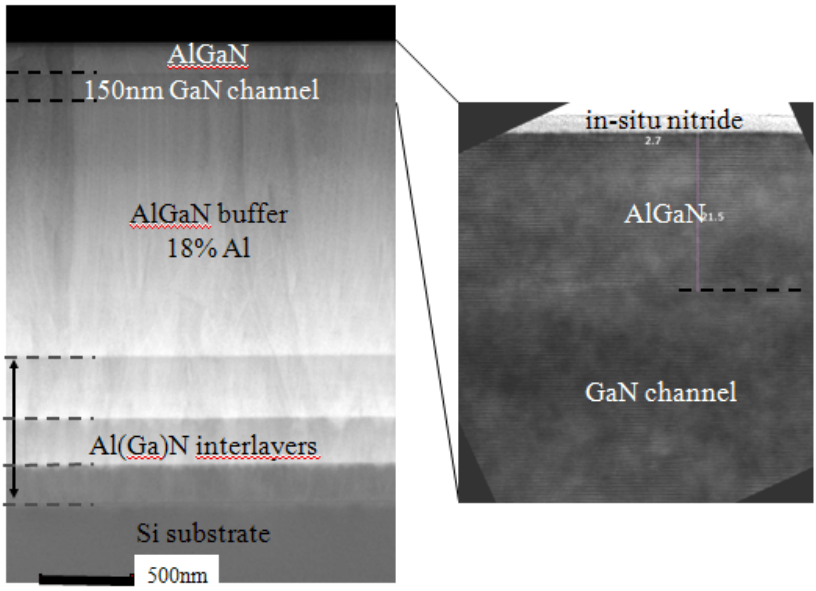


**Fig. 4.2** TEM of imec standard AlGaN/GaN/AlGaN DHFET. The top interfaces are very smooth.

grown as buffer layer followed by 150 nm of GaN as channel layer. Finally, 25 nm of $Al_{35\%}Ga_{65\%}N$ is grown as barrier layer and 3 nm of *in-situ* SiN as passivation layer. More details on the *in-situ* SiN passivation layer can be found elsewhere.[3,4] The growth temperature of the nitride layers in both structures was 1130°C. In this work, we use the DHFET structure for high-voltage applications due to the better electron confinement and the higher electric field of the AlGaN buffer layer. Figure 4.2 shows a TEM of the standard imec DHFET. More details on the epigrowth of the DHFET can be found in the work of Cheng *et al.*[2] Typical values of 2DEG mobility and channel concentration are 1400 $cm^2/V{\cdot}s$ and $1.45{\cdot}10^{13}$ $cm^{-2}$ for DHFET and about 1600 $cm^2/V{\cdot}s$ and $1.35{\cdot}10^{13}$ $cm^{-2}$ for SHFET. The sheet resistance is around 300Ω/square for both structures. The growth of nitride buffer layers on Si is challenging because of the large lattice and thermal mismatch between Si and III-nitride layers. This can lead to severe wafer bowing, epilayer cracking and even wafer breakage. A possible way to grow thick wafers with reasonable bow is the use of thick Si substrate as the CZ silicon. However, these samples

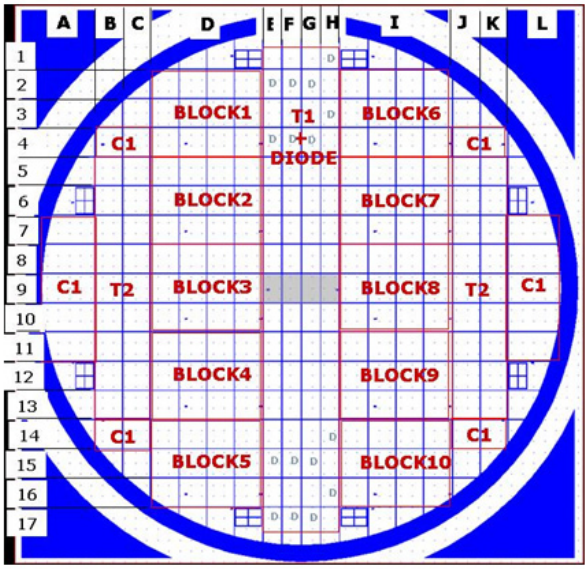


**Fig. 4.3** Overview of the PowerSwitch layout.

are not crack free and this can directly influence the breakdown. More details on the epigrowth of our structures can be found in the Ph.D. thesis of Cheng.[5]

## 4.2 Mask description

At the beginning of this work, a new mask, called "PowerSwitch", was designed. This mask is a 4 inch design for optical contact lithography. The full design consists of 8 layers: isolation, ohmic source and drain contacts, first interconnect level, gate, field plates, passivation opening (x2) and airbridges. An overview of the full design is shown in Fig. 4.3. The design contains the following structures:

- T1: Large transistors (144 fingers x 400 µm width) with 50 µm pitch
- T2: Large transistors (144 fingers x 400 µm width) with 100 µm pitch
- DIODE: Schottky diodes

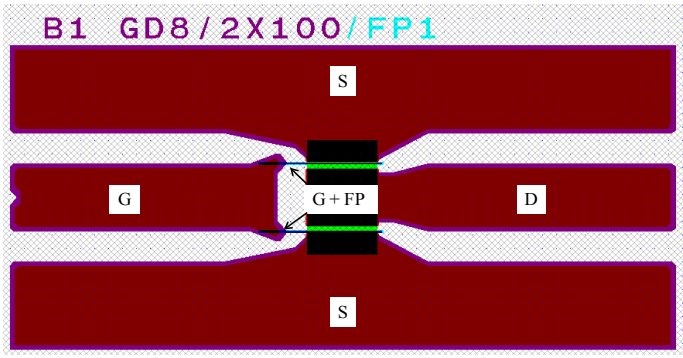


**Fig. 4.4** Top view of the "standard" small transistors.

- "BLOCKx": 10 identical blocks with small transistors (2 fingers x 100 µm width)
- Test structures and alignment marks

The devices investigated in this work are the small transistors located in 10 blocks on the entire wafer. Each block is identical and has in total 525 transistors divided in 21 cells. Each cell has 5 times 5 identical transistors if the field plate is not processed. With the field plate, each device column has 5 identical devices. Thus, five different field plate geometries are present in each cell. The advantage of this mask is that we can test devices with identical geometry on different places of the wafer. In this way we get information about the uniformity of the results on the entire wafer. Moreover, also the isolation structures, used to test the buffer quality, are located in each block. Therefore, the uniformity of the growth is also studied. The first cell of each block contains the "standard small transistor" shown in Fig. 4.4, which has the following dimensions:

- Number of fingers: 2
- Gate width: 100 µm
- Total gate width: 200 µm
- Gate length: 1.5 µm
- Source-Gate distance: 1.5 µm

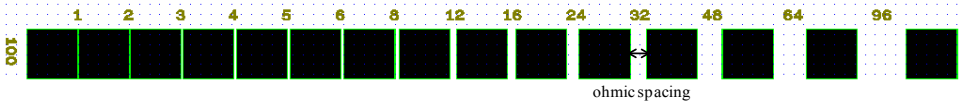


**Fig. 4.5** Top view of the isolation structures used to measure the buffer breakdown voltage. The ohmic spacing ranges from 1 µm to 96 µm.

- Gate-Drain distance: 8 µm

Variations are made in the field plate length (1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5 and 6 µm), the gate length (1, 1.5, 2 and 3 µm), the source-gate distance (1.5, 2, 2.5 and 3 µm), the gate-drain distance (5, 8, 10, 15 and 20 µm) and the gate width (2 × 50 µm, 2 × 100 µm, 2 × 200 µm, 2 × 400 µm and 2 × 600 µm). Each block also contains test structures for measuring others parameters such as ohmic contacts resistance, leakage path, 2DEG concentration and mobility, sheet resistance and buffer breakdown voltage. The structures for measuring the buffer breakdown voltage are shown in Fig. 4.5. The pads are formed by ohmic contacts separated by isolation. The distance between two consecutive pads varies between 1 µm to 96 µm. We call this distance "ohmic spacing". The width of each pad is 100 µm. The buffer leakage current and breakdown voltage is measured between two neighbouring contact pads.

## 4.3 Processing details

We will briefly describe the different processing steps. In particular, we will highlight the optimization done for some processing step which helped in reaching low leakage current and high breakdown voltage.

### 4.3.1 Device isolation

The first processing step is the device isolation. This can be done by "mesa" etching or nitrogen (N) implantation. Regarding the mesa etching, after exposure of the isolation mask, dry etching of the *in-situ* SiN, the top AlGaN layer, the GaN channel and part of the AlGaN buffer layer is done in an inductive coupled plasma source (ICP)

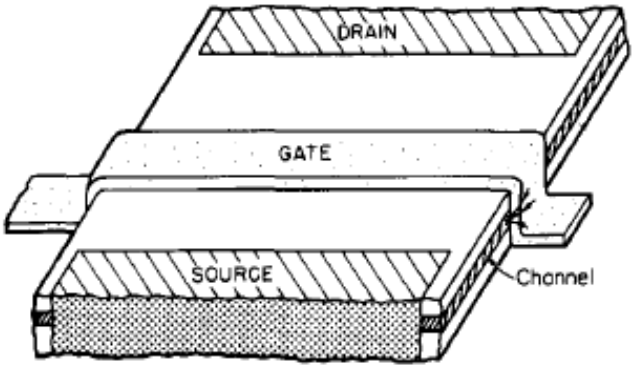


**Fig. 4.6** Perspective of HFET, showing the sidewall-leakage path at the gate-metal/mesa-sidewall overlap.[6]

etcher using $Cl_2$ chemistry. The optimized etching time was 5 minutes. The isolation pattern is etched deep into the AlGaN buffer layer. Chapter 5 will show that the breakdown voltage increases with the increase of the etching time. The disadvantage of the mesa etching is that in the isolated areas the surface is not protected by the in-situ SiN layer during the further processing steps. This can lead to unwanted impurities in the buffer layer and superficial damages. However, the main problem of devices isolated by the mesa etching is a gate leakage path where the gate metallization overlaps the exposed channel edge at the mesa sidewall as shown in Fig. 4.6.[6]

A good alternative to the mesa etching is the isolation by N implantation. The N implantation is done through the *in-situ* SiN passivation layer. The N ion beam destroys the lattice creating N and Ga vacancies. Simulations were performed with the SRIM program in order to optimize the dose and the energy of the implantation. Figure 4.7 shows the simulated vacancy concentration profile for two different energy/dose conditions. The red curve shows a shallow implantation up to the GaN channel/AlGaN buffer layer interface while the blue curve indicates a deep implantation into the AlGaN buffer layer. We studied the impact of shallow and deep implantation on the isolation resistance, on the buffer leakage current and on the buffer breakdown voltage. As shown in Fig. 4.8, the isolation resistance is on the order of $10^{13}$ Ω/square and is uniform on the

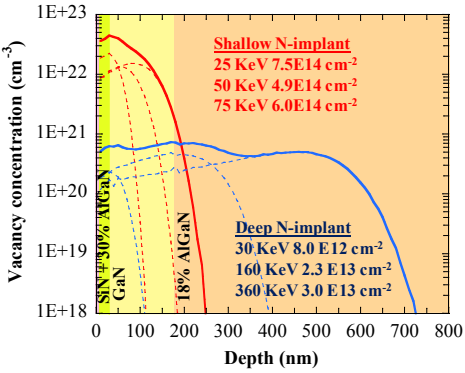


**Fig. 4.7** Simulations of the vacancy concentration profile for shallow (red curve) and deep (blue curve) N implantation.

entire wafer for a deep implantation. On the contrary, for the shallow implantation the isolation resistance is lower and is more spread over the wafer. In Chapter 5 we will show the effect of both shallow and deep implantation on the buffer leakage current and breakdown voltage.

We also studied the temperature stability of the implantation and of the mesa etching. As Fig. 4.9 shows, N implantation and mesa etching show the same thermal behaviour. The isolation resistance is stable up to 700°C and degrades at higher temperature. The temperature stability of the B implantation is also studied as possible alternative to N but this isolation resistance degrades even at temperatures as low as 500°C. Since the ohmic metal stack is annealed at 850°C the isolation is done after the ohmic contacts. Moreover, as we will show in Chapter 5, since the isolation done by the N implantation is less leaky compared to the mesa etching we decided to isolate the devices with the N implantation in our standard processing flow.

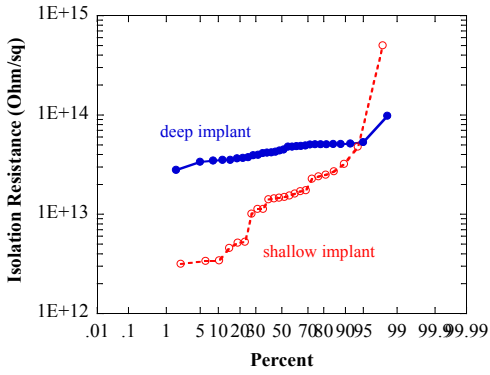


**Fig. 4.8** Isolation resistance in sample with shallow (red curve) and deep (blue curve) N implantation.

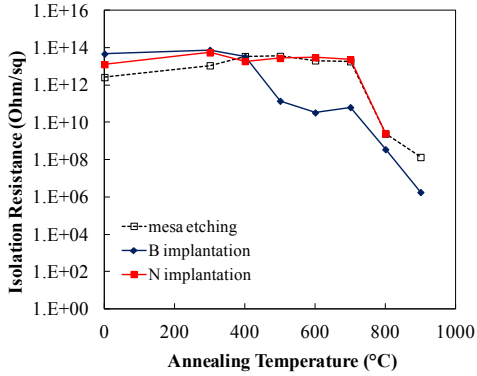


**Fig. 4.9** Thermal stability of the mesa isolation and of the nitrogen (N) and boron (B) implantation.

### 4.3.2 Source-Drain ohmic contacts

The formation of the Ohmic source-drain contacts, as is common practice in III-V processing, is done by "lift-off". First the photo is exposed, and then the SiN is dry etched using $SF_6$ chemistry in an ICP etcher. After this, Ti/Al/Mo/Au metal stack is

deposited. Next, the excess metal on top of the resist areas is "lifted-off" and a high temperature (~ 850 °C) rapid thermal anneal step is done to form low contact resistance source-drain pads. Typical contact resistance obtained for DHFETs is ~ 0.7 Ω·mm. As we mentioned above, the ohmic contacts are processed before the isolation step because of the high temperature budget. In samples with 50 nm of *in-situ* SiN passivation layer, the ohmic contacts are processed after dry etching this layer.

### 4.3.3 First interconnect layer

After device isolation and processing of the source- and drain contacts, the first interconnect level is processed. These metals stack uses 10/160/10 nm TiW/Au/TiW and is again patterned by lift-off. The TiW metal is used for its excellent adhesive properties, whereas gold (Au) results in low resistance values.

### 4.3.4 Gate

The processing of the gate level is the most critical step in the fabrication process, because of the small dimensions (1-1.5 μm), close to the limit of the optical contact lithography. We used a Schottky Ni/Au metal stack.

### 4.3.5 Passivation

To protect the devices from the environment 250 nm oxide is deposited as a passivation layer. In some experiments, SiN was also used but the optimization of the SiN deposition is still ongoing. After deposition, the passivation is opened above the bondpads. This is done using an $SF_6$ chemistry in an ICP dry etch tool.

### 4.3.6 Field plate

The field plate is formed by lift-off and 20/200 nm Ni/Au is used as metal stack. Afterwards, an extra passivation step was done.

Figure 4.10 shows the cross-section of the fabricated device and isolation structures.

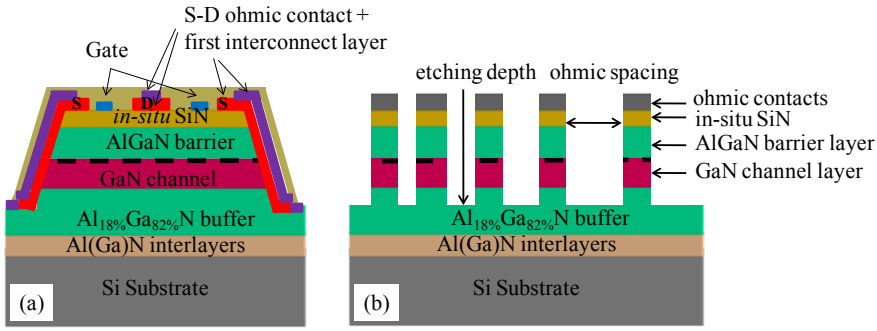


**Fig. 4.10** Cross-section of the fabricated device (a) and isolation structures (b). The top view is shown in Fig. 4.4 and Fig. 4.5.

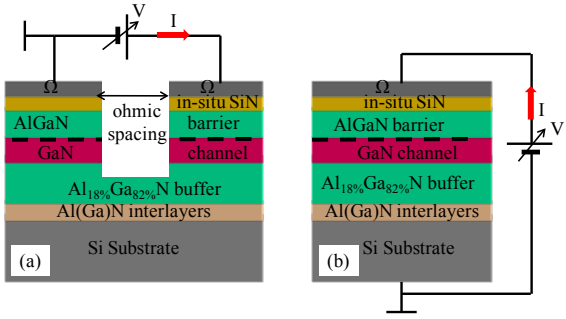


**Fig. 4.11** Measurement configuration of the horizontal (a) and vertical (b) buffer breakdown voltage.

## 4.4 Measurement configuration

During the high-voltage measurements the samples were characterized immersed in Fluorinert™, a high-electrical-strength fluid to avoid the arcing and tracking due to environmental conditions. The high-voltage characterization was performed on-wafer by using a Keithley 2410 test system up to 1100 V and a SHQ 222 ISEG power supply which can reach 6 kV. First, we measured the horizontal and vertical buffer breakdown voltage. The measurement configuration for the buffer breakdown voltage is shown in

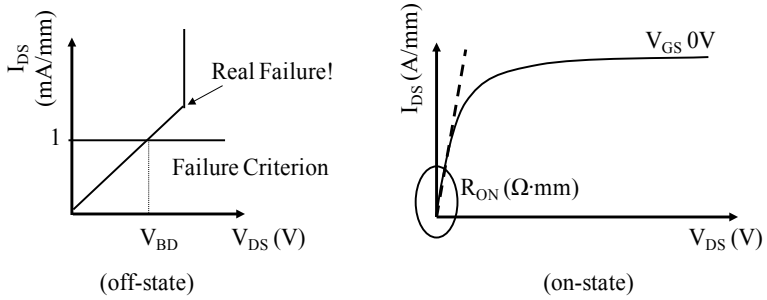


**Fig. 4.12** Off-state and on-state measurements of breakdown voltage and on-resistance, respectively. The breakdown voltage is measured when the drain leakage current reaches 1 mA/mm. The on-resistance is measured at low drain voltage when a $V_{GS}$= 0 V is applied.

Fig. 4.11. The buffer breakdown voltage is measured using the isolation structure shown in Fig. 4.10b for different ohmic spacing. The voltage was increased up till the buffer leakage current reached 1 mA/mm.

To measure the device breakdown voltage three terminals measurements were performed. The device, shown in Fig. 4.10a, was biased in the off-state. The gate was biased below pinch-off and the source was grounded. The drain-source voltage was ramped up till the drain leakage current reached 1 mA/mm as shown in Fig. 4.12. The on-resistance is measured in the on-state. It is extrapolated from the linear region of the $I_{DS}$-$V_{DS}$ characteristic measured at $V_{GS}$= 0 V as shown in Fig. 4.12. This value multiplied by the active device area gives the specific on-resistance ($R_{ON}A$).Moreover, the buffer and device breakdown are also measured with the electrical potential of the silicon substrate floating and grounded. We will discuss these measurements in Chapter 5.

## 4.5 References


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# Chapter 5

# Breakdown Mechanisms in The Buffer Layer Structure

In this chapter we study the breakdown mechanisms in the GaN-based buffer structures grown on Si substrate. We identified the Si substrate as the main limiting factor in achieving high breakdown voltage. Nevertheless, a buffer breakdown voltage as high as 1000 V is obtained. Several experiments are performed in order to optimize our buffer layer. We first investigate the impact of the isolation done with the mesa etching or the N implantation. In particular, we study the effect of both shallow and deep isolations. Then, the buffer breakdown voltage is studied as a function of the buffer thickness and of the Al content of the AlGaN buffer layer. In these experiments we used two different Si substrates: the highly doped CZ Si substrate and the highly resistive FZ Si substrate. Finally, we discuss the vertical buffer breakdown measurements as an alternative method to test the epilayer quality at high voltage. Table 5.1 lists the DHFET samples used in these experiments. We explained the epilayer structure in the previous chapter. The buffer thickness indicated in the table is the total epilayer thickness counting the AlN nucleation layer, the AlGaN intermediate layers and the AlGaN buffer layer. Fig. 4.5 and Fig. 4.10b, in the previous chapter, show the top view and the cross-section of the structures used for testing the buffer leakage current and breakdown voltage. Fig. 4.11 shows the measurement configurations for measuring the horizontal

**Table 5.1** DHFET samples used for the investigation of the buffer breakdown voltage.

| Sample | Substrate type | Buffer thickness (µm) | Al content of the AlGaN buffer layer (%) | Isolation |
|---|---|---|---|---|
| A1 | FZ | 1.4 | 8 | deep mesa |
| A2 | | 1.9 | | |
| A3 | | 2.5 | | |
| A4 | | 2.7 | | |
| A5 | | 3.1 | | |
| A6 | | 3.7 | | |
| A7 | | 4.3 | | |
| B1 | FZ | 1.9 | 18 | deep mesa |
| B2 | | 2.0 | | |
| B3 | | 2.6 | | |
| C1 | CZ | 2.0 | 18 | shallow N-implant |
| C2 | | 2.0 | 18 | deep mesa |
| C3 | | 2.0 | 18 | deep N-implant |
| C4 | | 2.9 | 18 | deep N-implant |
| C5 | | 3.1 | 18 | deep N-implant |
| C6 | | 4.0 | 18 | deep N-implant |
| C7 | | 4.6 | 18 | deep N-implant |
| D1 | CZ | 4.1 | 8 | deep mesa |

and vertical buffer breakdown voltage. The buffer leakage current is measured between two consecutive isolated ohmic pads and for different pad spacings.

## 5.1 Breakdown mechanisms in GaN-on-Si buffer layers

Theoretically, the buffer breakdown voltage of a planar isolation structure is determined by the ohmic spacing. Therefore, the buffer breakdown voltage should linearly increase with the ohmic spacing.[1] The behavior of the buffer breakdown voltage of the GaN buffer layer grown on Si substrate is different from the theoretical behavior as Fig. 5.1 shows. For GaN-on-SiC the buffer breakdown voltage linearly increases for all the ohmic spacings (region I). For GaN-on-Si two mechanisms are identified. For small ohmic spacing (< 5 μm) the breakdown voltage linearly increases (region I) being dependent on the ohmic spacing. For large ohmic spacing (> 5 μm) the buffer breakdown voltage saturates at a value as high as 1000 V (region II). We investigated this behavior by performing several experiments. Focused Ion Beam (FIB) images show that, in the isolation structure with small ohmic spacing, the structure breaks in the AlGaN buffer layer (Fig. 5.1-I), being dependent on the ohmic spacing. In the structure with large ohmic spacing, the buffer breakdown voltage is constant for all the ohmic spacing. Importantly, this behavior is found even if the buffer layer is grown on highly resistive Si substrate. Also, the value, at which the breakdown voltage saturates, depends on the thickness of the nitride buffer layer, being the voltage drop across Si negligible. Indeed, by increasing the thickness of the buffer layer we found that the saturated buffer breakdown voltage increases. We measured both the buffer breakdown voltage in the vertical direction grounding the Si substrate and the horizontal buffer breakdown with the Si substrate grounded. In both cases, we measured a value lower by a factor two compared to the horizontal value shown in Fig. 5.1 where the Si substrate is floating. This suggests a vertical double leakage current from the ohmic contacts into the Si substrate and a horizontal leakage current along the AlN/Si interface when the Si substrate is floating. When Si is grounded the current mainly flows in the vertical direction through the Si substrate. FIB images, performed on the isolation structure with large ohmic spacing, show that the structure breaks down in the Si substrate (Fig. 5.1-II), most likely at the Si interface where, due to the roughness of the interface, the distribution of the electric field is not homogeneous. This fact causes the saturation of the breakdown voltage at large ohmic spacing.

The vertical leakage current, from the ohmic contacts into the Si substrate and vice versa, can be explained by electron overflow into the buffer, possibly assisted by

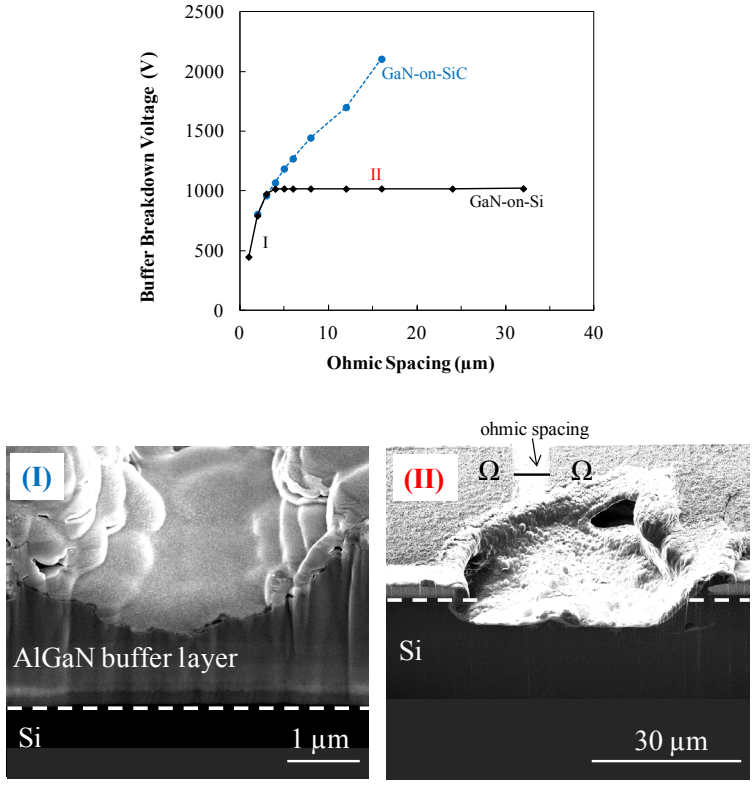


**Fig. 5.1** Buffer breakdown voltage in GaN-on-Si and GaN-on-SiC and Focused Ion Beam images in GaN-on-Si structures. Two breakdown mechanisms are identified in GaN buffer layer grown on Si substrate. (I) The breakdown voltage linearly increases with the ohmic spacing for small ohmic spacing (< 5 µm). The structure breaks in the buffer. (II) The breakdown voltage saturates for large ohmic spacing (> 5 µm). The structure breaks in the Si substrate. For SiC substrate the saturation of the breakdown voltage is not observed (only mechanism I).

electrically active threading dislocations. The horizontal leakage current path at the Si interface is due to Ga and Al doping and point defects which make the AlN/Si interface and the Si top layer highly conductive. In the growth of the nitride layers on Si substrate the growth of the AlN nucleation layer on top of Si is the most critical step because it affects the quality of the next buffer layers. The large thermal and lattice mismatch between Si and AlN leads to a severe amount of defects and, specially, of threading dislocations starting from the substrate and propagating through the entire buffer layers stack. These dislocations are responsible for the vertical leakage current. The defects along the interface are responsible for the horizontal leakage current. We found that they are electrically active and behave as deep acceptors. Spreading Resistance Probe (SRP) measurements are performed to investigate the conductivity of the Si substrate at the AlN/Si interface. In a highly resistive Si substrate, we measured a doping density of more than $10^{17}$ $cm^{-3}$ at the Si interface gradually decreasing 1 μm deep into the substrate. Thus, there is a localized region where the Si resistivity drops while in the rest of the substrate it remains unchanged as shown in Fig.7.1. This is mainly due to Ga atoms diffusing into the Si substrate during the MOCVD growth. They act as p-doping in Si. More details can be found in the work of Cheng.[2] Moreover, Ga atoms are not the only p-type impurity found in the Si top layer. By Electron Spin Resonance (ESR) measurements Si dangling bonds point defects ($P_b$) are measured at the AlN/Si interface, along the [111] direction normal to the AlN/Si interface and, more remarkable, along the other crystallographically equivalent <111> directions at angle 19° with the AlN/Si interface.[3,4] The presence of the 19° $P_b$ defects is an indication of a quite corrugated interface. These defects are electrically active and behave as deep acceptor. Also, a D-line, which indicates a certain amount of atomic disorder in the Si substrate, is measured. Therefore, these defects make our Si interface highly conductive. By interrupting this conductive layer by Si trench around the drain contact the breakdown voltage linearly increases with the ohmic spacing.[5]

The growth of thicker buffer layers is the most common technique for increasing the breakdown voltage of devices grown on Si.[6,7] However, the growth of thick buffer layers is challenging because of the large lattice and thermal mismatch between Si and III-nitride layers which can lead to severe wafer bowing, epilayer cracking and even wafer breakage. We grew thick buffer layer on thick CZ Silicon substrates that allow a better bow control. To reach high buffer breakdown voltage Ikeda *et al.* used a buffer

structure as thick as 7.3 µm together with the C-doping and a deep mesa etching.[6,8] We will also study the impact of the deep isolation done by both mesa etching and N implantation on breakdown voltage. However, instead of the growth thick buffer layer we proposed the Si removal technique for the enhancement of the breakdown voltage.[5,9]

## 5.2 Impact of the isolation: mesa etching and N implantation

We studied the impact of the isolation processing on buffer leakage current and on buffer breakdown voltage. In Chapter 4 we described the processing steps for the fabrication of the structures for studying the buffer. The most important steps which can influence the buffer leakage current are the isolation and the fabrication of the ohmic contacts. The isolation of our structures is done by mesa etching or by N implantation and the ohmic metal stack is annealed at 850ºC. In Chapter 4, Fig. 4.8 shows the thermal stability of both mesa etching and N implantation. In both cases the isolation resistance degrades after the sample is annealed at 800ºC. The consequence is that the buffer structure becomes leaky. If the isolation is done after annealing the ohmic contacts, the buffer structure is less leaky and the buffer breakdown voltage is higher. Thus, the first important conclusion was that the ohmic contacts have to be processed before the isolation.

### 5.2.1 Depth of mesa etching and N implantation

Second, the impact of the mesa etching and of the N implantation depth on the buffer structure was investigated. We used the sample A4 to investigate the impact of different mesa etching times. As described in Chapter 4, the mesa etching isolation is done in an ICP etcher. By setting the etching time it is possible to control the etching depth. Figure 5.2 shows that after etching for 1 minute only the *in-situ* passivation, the AlGaN barrier and part of the GaN channel is etched away. After 5 and 10 minutes the structure is etched deep into the AlGaN buffer layer. We define MET1, MET5 and MET10 the samples with the etching time of 1 minute, 5 minutes and 10 minutes, respectively. Figure 5.3 shows the buffer breakdown voltage and the buffer leakage current measured on these samples. The buffer breakdown voltage is about 720 V in the sample MET1 with a shallow mesa while it is about 900 V and independent of the ohmic

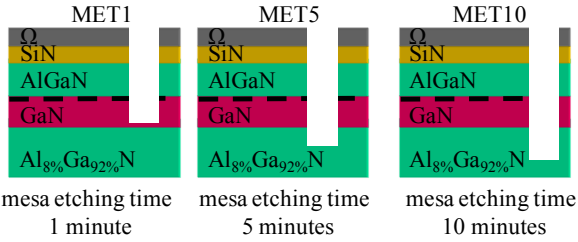


**Fig. 5.2** On sample A7 three different mesa etching times were studied. Sample MET1, MET5 and MET10 were etched 1 minute, 5 minutes and 10 minutes, respectively.

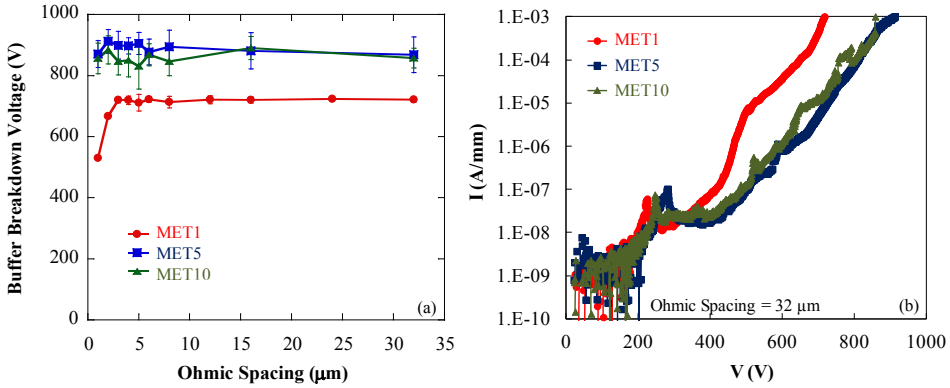


**Fig. 5.3** Buffer breakdown voltage (a) and buffer leakage current (b) in the samples MET1, MET5 and MET10.

spacing for samples MET5 and MET10 with a deep mesa. By etching deep into the AlGaN buffer layer the buffer leakage current at high voltages is reduced and a buffer breakdown voltage as high as 900 V could be achieved as shown in Fig.5.3b. In samples MET1 with shallow mesa, the buffer breakdown voltage reaches a maximum value for an ohmic spacing > 4 µm while on the samples MET5 and MET10 with deep mesa it is constant and independent of the ohmic spacing. From Focused Ion Beam (FIB) images shown in Fig.5.4 it can be seen that if the isolation etch is deep enough into the AlGaN buffer layer the structure breaks down in the Silicon (Fig.5.4a, b) for all ohmic spacings.

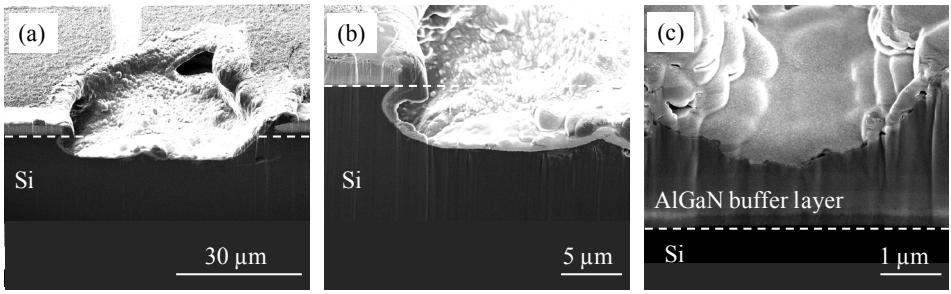


**Fig. 5.4** Images by Focused Ion Beam: buffer breakdown in sample MET5 (deep mesa) with ohmic spacing of 5 µm (a); magnification of the left part of Fig. 5.4a (b); buffer breakdown in sample MET1 (shallow mesa) with ohmic spacing of 1 µm (C).

This explains the constant breakdown voltage. If the isolation etch is not deep enough, the structure breaks down in the buffer layer for small ohmic spacing (Fig.5.4c) and the breakdown voltage increases with increasing the ohmic spacing up to 4 µm. For ohmic spacing larger than 4 µm the structure breaks in the Si substrate as for the sample MET5 and MET10. By increasing the etching time from 5 to 10 minutes the buffer breakdown voltage and the buffer leakage current are not affected.

The same behavior is obtained if the structure is isolated with the N implantation. We used the samples C1, C2 and C3. In sample C1 the N implantation is shallow, in sample C2 the isolation is done with a deep mesa and in sample C3 the N implantation is deep. In Chapter 4, Fig. 4.7 shows the conditions and the depth of the N implantation. With the shallow implantation, the structure is implanted till the GaN channel/AlGaN buffer layer interface. Instead, with the deep implantation, the isolation is deep into the AlGaN buffer layer. The isolation resistance obtained with the deep N implantation is higher and uniform on the entire wafer compared to the one obtained with the shallow implantation (Fig. 4.8). Figure 5.5 shows the buffer breakdown voltage and the buffer leakage current measured in the samples C1, C2 and C3. As for deep mesa etching, the structure with the deep N implantation C3 (green curve) shows a buffer breakdown voltage higher than the structure with the shallow implantation C1 (red curve).

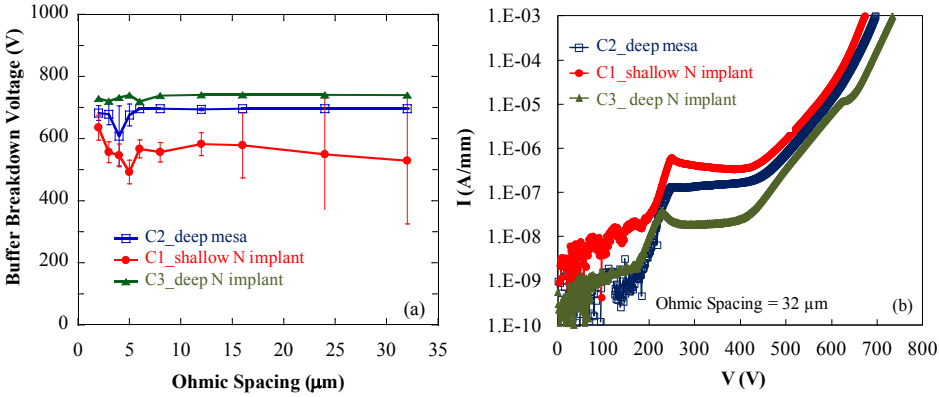


**Fig. 5.5** Buffer breakdown voltage (a) and buffer leakage current (b) in the samples C1, C2 and C3 with shallow N implantation, deep mesa and deep N implantation, respectively.

Also, these data are very spread at large ohmic spacings. Moreover, in the Fig.5.5b, the buffer leakage current in C3 is about two orders of magnitude lower than in sample C1. This is a direct consequence of the better isolation resistance obtained with the deep implantation. Fig. 5.5a also shows that the buffer breakdown voltage obtained in sample C3 with a deep N implantation is slightly better than in sample C2 (blue curve) where the isolation is done with the deep mesa. Also, sample C2 is leakier than sample C3 as shown in Fig. 5.5b. This is probably due to the fact that the buffer structure, isolated with the implantation, is protected by the *in-situ* passivation layer so impurity and superficial damages can be reduced compared to the structure isolated with the mesa etching.

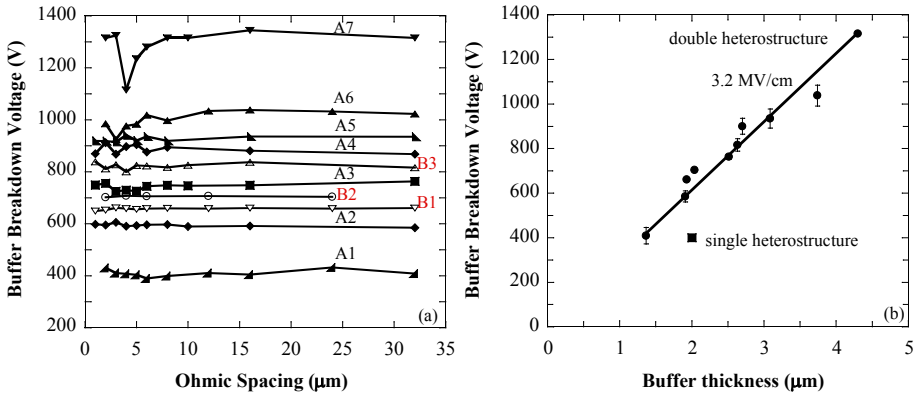


**Fig. 5.6** Buffer breakdown voltage versus ohmic spacing in samples A and B (a). The Al content of the AlGaN buffer layer is 8 % and 18 % in the A and B series, respectively. The buffer breakdown voltage linearly increases with the buffer thickness with a slope of 3.2 MV/cm. (b).

## 5.3 Impact of the buffer thickness and of the Al content in the AlGaN buffer layer

The value at which the buffer breakdown voltage saturates is dominated by the nitride epilayer thickness. To study the impact of the buffer thickness on buffer breakdown voltage more in detail we used seven samples with a buffer thickness ranging from 1.4 µm up to 4.3 µm. These samples are listed in Table 5.1 and belong to the A serie. These samples are grown on a higly resistive Float Zone Si substrate and the Al concentration of the AlGaN buffer layer is 8 %. To study the impact of the Al concentration of the AlGaN buffer layer we used three samples of the B serie with 18 % Al concentration. The isolation of all these samples is done with the deep mesa etching. Figure 5.6 shows the buffer breakdown voltage measured on all samples of the A and B series. The buffer breakdown was found to be dependent on the thickness and the Al concentration of the AlGaN buffer layer. For both groups of samples A and B, the buffer breakdown increases with the buffer thickness. Moreover, for the same buffer thickness

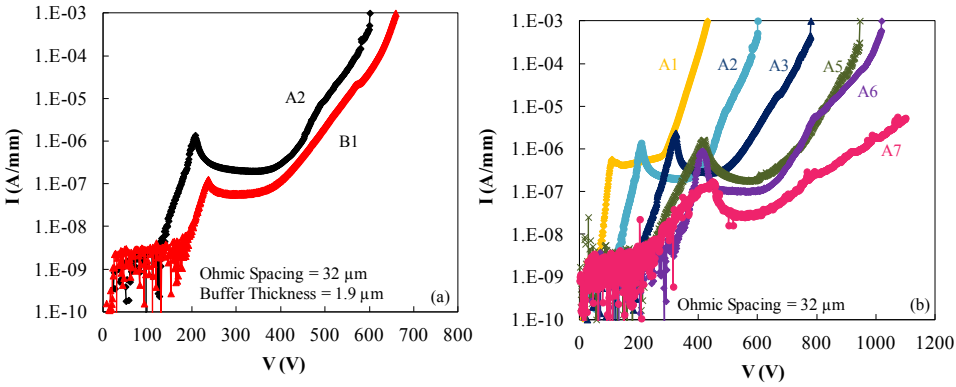


**Fig. 5.7** Buffer leakage current in samples A2 and B1 with the same buffer thickness and different Al content in the AlGaN buffer layer (a). Buffer leakage current of samples A with 8% of Al content in the AlGaN buffer layer (b). The measurement of sample A7 was limited by the Keithley 2410 which has a voltage limit of 1100 V.

(for example 1.9 µm) the sample B1 with Al concentration of 18 % results in a higher buffer breakdown compared to sample A2 with only 8 % of Al concentration (Fig. 5.6a) Therefore, the thicker the buffer and the higher the Al concentration in the AlGaN layer, the higher is the buffer breakdown voltage. This trend is visualized in Fig. 5.6b. A linear relationship with a 3.2 MV/cm slope was extracted. Moreover, the graph clearly shows that the values for the DHFETs are considerably higher compared to SHFETs with identical total buffer thickness: only 400 V was measured in the SH structures with 2 µm thick buffer while 600 V is achieved in the DH structure. As can be seen in Fig. 5.6a, the buffer breakdown is independent on the ohmic spacing. As we have already discussed in the previous paragraph, if the mesa isolation is deep enough into the AlGaN layer the structure breaks down in the Silicon substrate even for the small ohmic spacings resulting in a buffer breakdown independent on the specific ohmic spacing. Figure 5.7a shows that the use of 18 % AlGaN buffer layer (sample B1) results in lower leakage compared to the AlGaN buffer layer with 8 % (sample A2). This is not due to an improvement of the electron confinement because, as was shown in Fig 3.16, the confinement does not change if the GaN channel is 150 nm thick. The higher band gap and critical electric field of the AlGaN with 18 % Al content are responsible for the

lower leakage current and the higher buffer breakdown voltage. Figure 5.7b shows the buffer leakage current in the samples A. By increasing the buffer thickness up to 3.1 µm the buffer leakage current is reduced and a current bump appears at higher voltages. From 3.1 µm buffer thickness on, the position of this current bump does not change with the increase of the buffer thickness and the decrease of the buffer leakage current is more significant. We will investigate the current bump in more detail in Chapter 7.

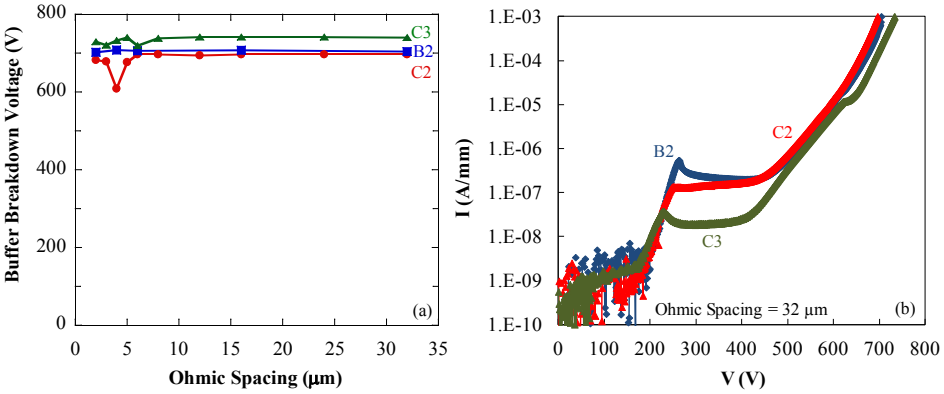


**Fig. 5.8** Buffer breakdown voltage (a) and buffer leakage current (b) of samples B2, C2 and C3. The buffer thickness is 2 µm, the Al concentration in the AlGaN buffer layer is 18%. The isolation is done with the deep mesa in C2 and B2 and deep N implantation in C3.

## 5.4 Float-Zone vs. Czochralski Silicon substrate

In order to grow thick nitride buffers on top of Si substrates with low wafer bow thick CZ Si substrates were used. More details on the epigrowth can be found in the Ph.D. thesis of Cheng.[2] This substrate is highly-doped compared to FZ Si substrate. Therefore, we also studied the impact of the Si resistivity on breakdown voltage. Table 5.1 shows the samples grown on CZ Si substrate. The thickest sample is C7 with a buffer thickness of 4.6 µm and 18 % of Al content in the AlGaN buffer layer. On FZ Si substrate the thickest buffer is 4.3 µm with 8 % of Al content.

We first studied the impact of CZ Si substrate on buffer breakdown voltage and leakage current. We compared sample B2, grown on FZ Si, with C2 and C3, grown on CZ Si. They have the same buffer thickness and Al content in the AlGaN buffer layer. The isolation is done with deep mesa etching for B2 and C2 and with deep N implantation for C3. Figure 5.8a shows the buffer breakdown voltage and Fig. 5.8b the buffer leakage current. The buffer breakdown voltage is around 700 V in the samples B2

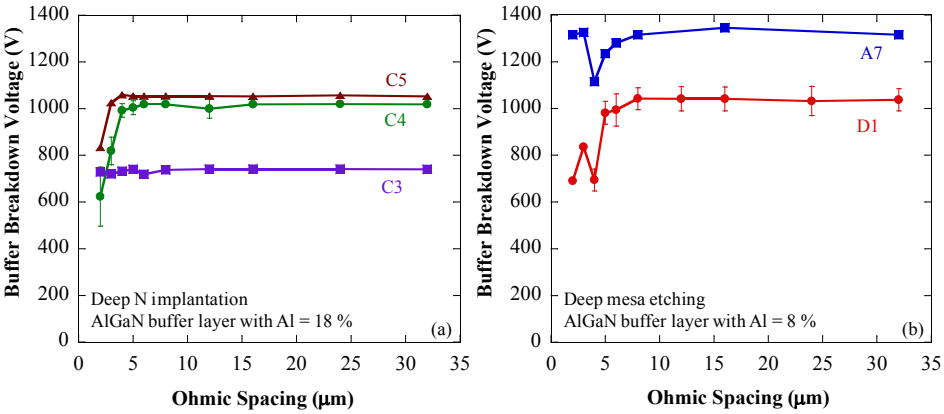


**Fig. 5.9** Buffer breakdown voltage in samples C3, C4 and C5 with a buffer thickness of 2.0 µm, 2.9 µm and 3.1 µm, respectively (a); and in samples D1 and A7 with a buffer thickness of 4.1 µm and 4.3 µm, respectively.

and C2. It is slightly higher (~ 740V) in sample C3 because of the implantation as we discussed previously. Sample B2 grown on FZ Si and sample C2 on CZ Si show the same buffer breakdown voltage. The buffer leakage current is even comparable. Sample C3 shows a lower leakage current due to the deep N implantation. The important conclusion is that the buffer breakdown voltage is not affected by the resistivity of the Si substrate.

We also studied the impact of thick buffers grown on CZ substrate on buffer breakdown voltage. Figure 5.9a shows that the buffer breakdown voltage increases with the buffer thickness from 740 V up to 1050 V for a buffer thickness ranging from 2 µm up to 3.1 µm. Thus, the same behavior for the samples grown on FZ Si substrates is found. Figure 5.9b shows the buffer breakdown voltage for a buffer thickness of 4.1 µm (sample D1) and 4.3 µm (sample A7) and for an Al content of 8%. The buffer breakdown voltage increases up to 1350 V by increasing the buffer thickness up to 4.3 µm. Sample D1 shows a buffer breakdown voltage comparable with samples C4 and C5 despite the thicker buffer. This is attributed to the different isolation and Al content of

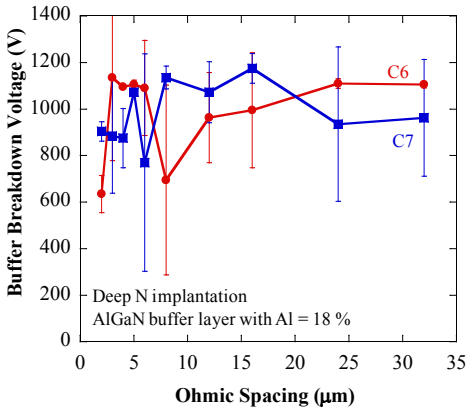


**Fig. 5.10** Buffer breakdown voltage in samples C6 and C7 with a buffer thickness of 4.0 µm and 4.6 µm, respectively. Data are very spread due to several cracks in the epilayer structure.

the AlGaN buffer layer. Thus, a direct comparison between D1, C4 and C5 is not possible.

On CZ substrates buffers thicker than 4 µm and with 18% of Al content in the AlGaN buffer layer are grown. However, these structures show several cracks. Indeed, the buffer breakdown voltage data are very spread as can be seen in Fig. 5.10. This shows that, by using the imec growth parameters available at that time, 4 µm is the upper limit for the buffer thickness. However, the growth of thick nitride buffer layer on Si with high breakdown voltage is possible as shown by Ikeda *et al.*[6] They grew a GaN buffer layer as thick as 7.3 µm reaching a buffer breakdown voltage as high as almost 2000 V for an ohmic spacing of 32 µm[6].

In the experiments described above the Si substrate potential is floating. If the substrate is grounded the buffer breakdown voltage is half of the value obtained with the Si substrate floating. This proves that the buffer leakage current vertically flows down

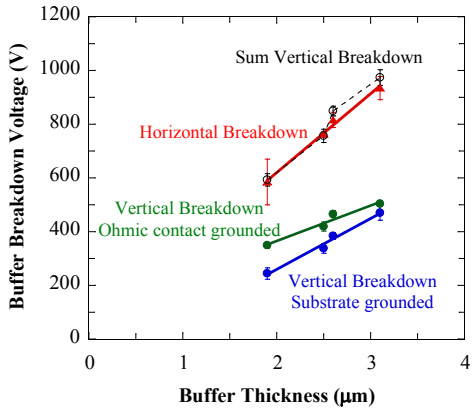


**Fig. 5.11** Buffer breakdown voltage measured in vertical direction with the ohmic contact grounded (green curve) or with the Si substrate grounded (blue curve). The sum of these values (black curve) is the same as the buffer breakdown voltage measured in the horizontal direction (red curve).

into the Si substrate and along the AlN/Si interface which breaks earlier due to the lower critical electric field compared to that one of the nitride epilayers.

## 5.5 Vertical high voltage buffer breakdown measurements

In order to test the quality of the nitride buffer layers grown on Si by using the high-voltage electrical characterization we measured the buffer leakage current in the vertical direction. The vertical leakage current is measured applying a positive drain bias on top of the ohmic contact and grounding the Si substrate as shown in Fig. 4.10b and vice versa. The samples used in this experiment are A2, A3, A5, A7 and B3. Figure 5.11 shows that the vertical buffer breakdown voltage is lower than the horizontal one. The difference is almost a factor 2. The value measured with the ohmic contact grounded (green curve) is slightly higher than the value measured with the Si substrate grounded (blue curve). The sum of these values perfectly matches the buffer breakdown voltage measured in the horizontal direction with the Si substrate floating. Figure 5.11 also shows that by increasing the thickness of the nitride buffer layers the vertical breakdown

voltage increases as the horizontal buffer breakdown shown in Fig. 5.6. A slope of 1.6 MV/cm was extrapolated, which is a factor 2 lower compared to the one mentioned above in the horizontal direction. This shows that the limiting factor to achieve high breakdown voltages is the low breakdown field of Si at the AlN/Si interface (0.3 MV/cm) and thus as thick as possible buffers are needed. The ‘‘average’’ buffer Al concentration for all epilayers studied is almost 35%. The intrinsic material critical electric field, interpolated between the 3.3 and 11.7 MV/cm values for GaN and AlN respectively, would then be around 6.2 MV/cm. This is only a factor 4 higher than our experimental value (1.6 MV/cm). This discrepancy can be attributed to the high dislocation density ($10^9$ $cm^{-2}$) in the buffer layers due to the large lattice mismatch between the III–nitrides and the Si substrate. Moreover, increasing the thickness of the nitride buffer layers the vertical buffer breakdown voltage measured in both configurations becomes the same, which is exactly half of the horizontal value.

The vertical leakage current is shown in Fig. 5.12. When the bias is applied on the ohmic contact and the substrate is grounded (blue curves) the leakage current increases faster compared to the leakage current measured with the ohmic contact grounded and the bias applied at the Si substrate (green curve). Also, this vertical leakage current decreases with the increase of the epilayer thickness. The current bump appears only when the structure is biased on the Si substrate. We will explain this in Chapter7.

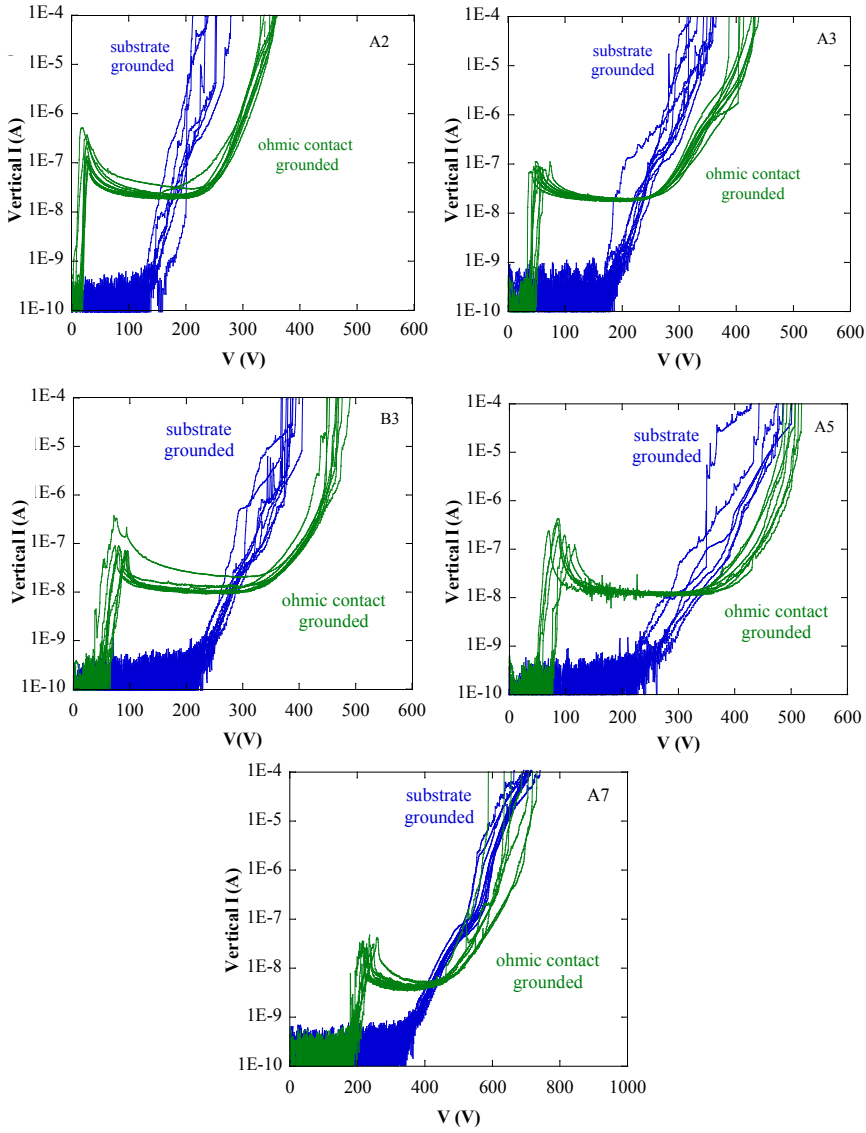


**Fig. 5.12** Buffer leakage current in samples A2, A3, B3, A5 and A7 with a buffer thickness of 1.9 µm, 2.5 µm, 2.6 µm, 3.1 µm and 4.3 µm, respectively. The difference between the breakdown values measured with substrate grounded or ohmic contact grounded decreases with the buffer thickness.

## 5.6 References


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# Chapter 6

# Analysis Of The Device Breakdown Voltage

In this chapter we will discuss the breakdown of GaN-on-Si devices. The device breakdown voltage exhibits the same behaviour as the buffer breakdown voltage discussed in the previous chapter. For small gate-drain distances ($L_{GD}$) it linearly increases being dominated by the device geometry. For large $L_{GD}$ it saturates at a certain voltage determined by the buffer thickness. In order to increase the breakdown voltage we will discuss the impact of the gate-connected field plate and of the buffer thickness. Moreover, we performed high voltage simulations of AlGaN/GaN devices with and without Si substrate to understand the breakdown mechanisms. We propose the Si substrate removal as a viable technique for enhancing the breakdown voltage. Finally, we will also discuss our first approach in the fabrication of enhancement mode devices. However, we will point out on the behavior of the device breakdown voltage which, as for the depletion mode devices, saturates at large $L_{GD}$.

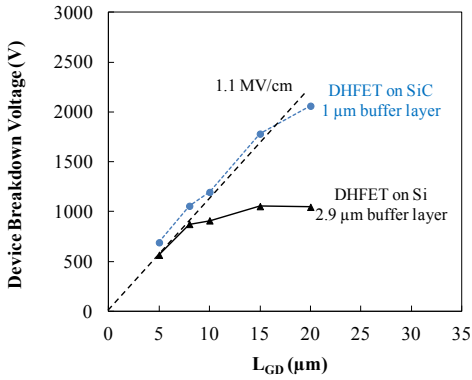


**Fig. 6.1** Breakdown voltage of devices fabricated on buffer layer grown on SiC (blue line) and on Si (black line). The device breakdown voltage saturates for devices fabricated on buffer layers grown on Si substrate. On the contrary, it increases with $L_{GD}$ for SiC substrate. The relationship is linear with a slope of 1.1 MV/cm.

## 6.1 Breakdown mechanisms in GaN-based devices

For planar devices the most important parameter, that impacts the high breakdown voltage, is the distance between the gate and drain contacts ($L_{GD}$). By increasing this distance the electric field decreases and consequently higher breakdown voltage values can be reached.[1,2] This behavior is nicely shown by our devices fabricated on a buffer layer grown on SiC substrate. Instead, for Si substrate the device breakdown voltage saturates as shown in Fig. 6.1. The linear relationship between device breakdown voltage and gate-drain distance is 1.1 MV/cm for SiC substrate and also for Si substrate in the linear region. The value at which the device breakdown voltage saturates linearly increases with the thickness of the buffer layer, as is also reported by several people.[3,4,5] Moreover, the device breakdown voltage measured with the Si substrate grounded is half of the value measured with the Si substrate floating. This result, as for the buffer structure, suggests a double vertical leakage current into the Si and a horizontal leakage current along the Si interface, which limit the breakdown voltage. Also, the device

breakdown voltage of about 1000 V for devices with $L_{GD}$ = 15 µm and 20 µm is the same as the buffer breakdown voltage for large ohmic spacing. This is a further confirmation of the fact that also the device breakdown voltage is limited by the low critical electric field of Si. It is well known that the device breakdown voltage increases if a field plate is connected either to the gate or to the source. As we discussed in Chapter 3, an optimized field plate alleviates the electric field peak at the gate edge on the drain side and consequently the device breakdown voltage increases. As we will show in the next paragraphs, the field plate increases the device breakdown voltage more than a factor two, but only for devices with short gate-drain distances. In the devices with large gate-drain distance the increase of the device breakdown voltage is only about 10 %. This confirms that the main limitation in achieving high device breakdown voltage in devices with large $L_{GD}$ is not the electric field peak at the gate edge.

We performed high voltage simulations of AlGaN/GaN devices with and without Si substrate with different gate-drain distances. The high voltage simulations of AlGaN/GaN/Si devices show that the impact ionization factor is higher at the Si interface where it breaks independently of the gate-drain distance in the saturation region. To increase the device breakdown voltage at large $L_{GD}$ we propose the Si removal technique. After removal of the Si substrate, the breakdown voltage linearly increases with the gate-drain distance.[6,7,8]

Moreover, the off-state drain leakage current shows a current bump at high voltage similar to that one seen in the buffer leakage current in Fig. 5.7. This is a further confirmation of the fact that the drain leakage current has a leakage current component which flows from the surface into the Si substrate and along the AlN/Si interface. As will be explained in Chapter 7, the current bump is due to a mechanism of charging and discharging of deep defects in the Si at the AlN/Si interface.

**Table 6.1** DHFET-based devices with different $L_{GD}$ and $L_{FP}$.

| Gate-drain distance ($L_{GD}$) (µm) | Field plate length ($L_{FP}$) (µm) |
|---|---|
| 2 | 1 |
| 3 | 1 |
| 5 | 1-1.5-2-2.5-3 |
| 8 | 1-2-3-4-5-6 |
| 10 | 1-2-3-5-7 |
| 15 | 1-3-5-7-9 |
| 20 | 1-2-3-5-10 |

## 6.2 Effect of the field plate on breakdown voltage and on-resistance

In Chapter 3 we described the field plate technique and we studied the impact of the field plate geometry on the AlGaN surface electric field.[9] The field plate extends the depletion region creating a second peak at the field plate edge and reducing the electric field peak at the gate edge. Thus, the breakdown voltage of the device increases. For studying the impact of the field plate on breakdown voltage and on-resistance we used a standard epilayer structure with a total buffer thickness of 2 µm. The isolation was done by deep mesa etching. Based on the simulations reported in Chapter 3, we used an in-situ SiN passivation layer as thick as 100 nm. The gate is processed after dry etching the SiN. The field plate is connected to the gate and is on top of the in-situ SiN. As we explained in Chapter 4, for each device with a certain $L_{GD}$ there are five different field plate geometries in the PowerSwitch mask. The devices used in this experiment are listed in Table 6.1. In this experiment the electric potential of the silicon substrate was floating.

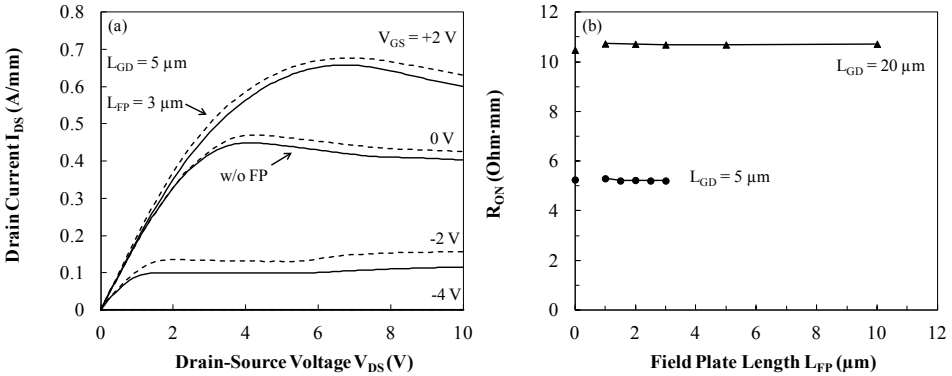


**Fig. 6.2** $I_{DS}$-$V_{DS}$ characteristics at different gate voltages without field plate and with 3 µm field plate length (a). On-resistance as a function of the field plate length (b).

DC measurements were performed on devices with and without field plate before measuring the breakdown voltage. Fig. 6.2a shows the DC drain-source current ($I_{DS}$) - voltage ($V_{DS}$) characteristics at different gate voltages without field plate and with a field plate length of 3 µm in a device with $L_{GD}$= 5 µm. The maximum $I_{DS}$ slightly increases with the field plate and reaches about 680 mA/mm at $V_{GS}$= 2 V and the devices exhibit a pinch-off voltage of -4 V with and without field plate. For each device the on-resistance was measured for each field plate length reported in Table 6.1. Fig. 6.2b shows the on-resistance for $L_{GD}$= 5 µm and 20 µm with and without field plate. The on-resistance is constant with the field plate length as expected. Same behavior was observed for all the other devices. Before measuring the device breakdown voltage we tested the buffer breakdown voltage. For all the ohmic spacings this was 700 V as expected for a buffer thickness of 2 µm, as we discussed in the previous chapter. The device breakdown voltage without field plate is shown in Fig. 6.3. Also for the device breakdown voltage two mechanisms are identified. For small gate-drain distances ($L_{GD}$ < 8 µm) the breakdown voltage linearly increases with the gate-drain distance, being dominated by the device geometry. For 8 µm < $L_{GD}$ < 20 µm the breakdown saturates at about 600 V. As we discuss previously, this behavior is due to a double leakage current between the metal contacts and the silicon substrate and along Si which cause device breakdown at

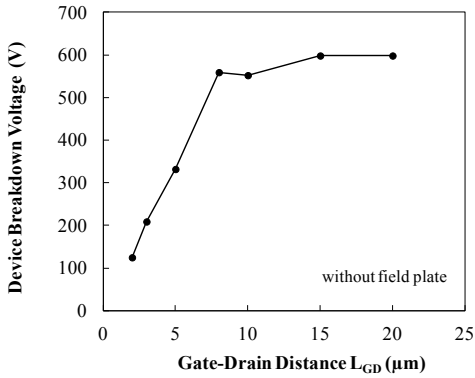


**Fig. 6.3** Device breakdown voltage without field plate.

the AlN/Si interface due to the lower breakdown field of Si compared to III-nitride layers. Figure 6.4a shows the device breakdown voltage for the different field plate lengths reported in Table 6.1. Devices with $L_{GD}$=5 µm, 8 µm and 10 µm shows a higher breakdown voltage with $L_{FP}$=1 µm. Instead, devices with $L_{GD}$=15 µm and 20 µm show a comparable breakdown voltage for all the field plate lengths. From a capacitance point of view, the shortest field plate length is preferable. Also, for such field plate length, according to simulations in Chapter 3, the electric field peak at the field plate edge is comparable with the one at the gate edge. Fig. 6.4b shows the direct comparison between the breakdown voltage in devices without FP and with 1 µm $L_{FP}$. For devices with short $L_{GD}$ the breakdown voltage is increased by more than a factor 2. This result indeed confirms that the breakdown mechanism is dominated by the device geometry. For devices with long $L_{GD}$ ($L_{GD}$ > 8 µm) the increase is only about 10% because the breakdown is limited by the silicon substrate. Moreover, capacitance measurements in the on-state ($V_{GS}$= 0 V) were carried out on devices without and with field plate as shown in Fig. 6.5. We measured the total gate capacitance on a device with $L_{GD}$ = 8 µm and with the different field plate lengths listed in Table 6.1. The source and drain ohmic contacts were grounded and the $V_{GS}$ was biased at 0 V with 100 mV of AC magnitude and a frequency of 1 MHz. As expected, the capacitance increases with the field plate length, for $L_{FP}$ = 1 µm the increase is only 35%.

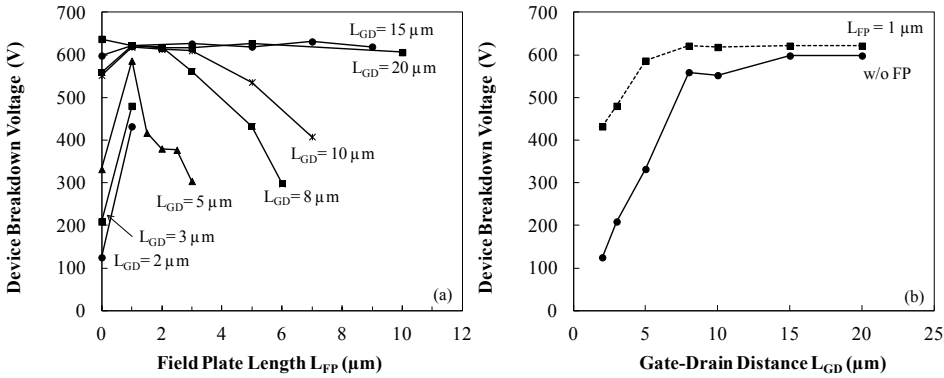


**Fig. 6.4** Device breakdown voltage as a function of the field plate length (a). Device breakdown voltage without field plate and with 1 µm field plate length (b).

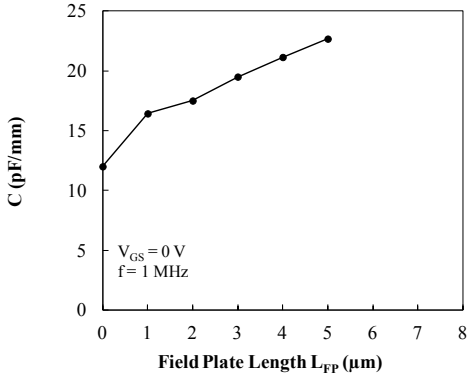


**Fig. 6.5** Total capacitance measured in a device with $L_{GD}$= 8 µm.

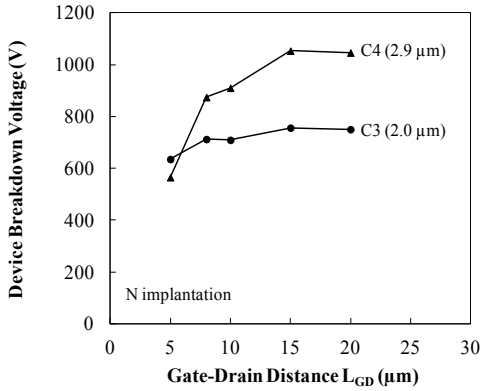


**Fig. 6.6** The device breakdown voltage increases with the increase of the buffer thickness. The buffer thickness is indicated in brackets. The maximum value is plotted.

## 6.3 Impact of the buffer thickness on the device breakdown voltage

In this paragraph we study the effect of the buffer thickness on the device breakdown voltage. Figure 6.6 shows the device breakdown as a function of $L_{GD}$ measured in samples C3 and C4, listed in Table 5.1. We fabricated the devices following the standard processing described in Chapter 4. The device breakdown voltage shows the same behavior as the buffer breakdown voltage. It increases with the thickness of the buffer layer. A breakdown voltage higher than 1000 V was achieved in the sample C4 with a buffer thickness of only 2.9 µm and 760 V in the sample C3 with a buffer thickness of 2.0 µm. However, it is important to mention that the increase of the device breakdown voltage with the buffer thickness is found also in the devices fabricated on the buffer layer of the A series where the Si substrate used is the highly resistive Float Zone. Therefore, the saturated device breakdown voltage is dominated by the thickness of the buffer layer being the voltage drop across Si negligible. The lower critical electric field of the Si substrate is the limiting factor in achieving high breakdown voltage. We studied the uniformity of these results on the entire wafer. Figure 6.7 shows the device breakdown voltage distribution measured in devices with different gate-drain distances

on the entire wafer. For each $L_{GD}$ we measured 50 devices. The median and the maximum value were extrapolated and plotted in Fig. 6.7a and Fig. 6.7c. The distribution is plotted in Fig. 6.7b and Fig. 6.7d. Sample C3 with a buffer thickness of 2 µm shows a better uniformity compared to sample C4 with 2.9 um as buffer thickness. Importantly, in both samples the highest device breakdown voltage is comparable with the buffer breakdown voltage. Figure 6.8 shows the drain leakage current of several devices with $L_{GD}$ = 20 µm measured in sample C3. The leakage current is as low as $10^{-8}$ A/mm. The same current bump measured in the buffer leakage current is detected in the off-state drain leakage current at about 300 V. We will discuss the origin of the current bump in the next chapter.

In the high voltage characterization of the devices discussed so far, the potential of the Si substrate is floating. We also tested the device breakdown voltage with the Si substrate grounded. We found the same behavior as the buffer breakdown voltage. The device breakdown voltage with the Si substrate grounded decreases of a factor 2, confirming that the main leakage current is vertically down to the Si substrate and horizontally along the Si interface.

In Chapter 4 we described the PowerSwitch mask as a dedicated mask for studying the impact of the device geometries on breakdown voltage. We measured the device breakdown voltage in devices with different gate widths, source-gate distances and gate lengths. The device breakdown voltage was comparable to the values reported in Fig. 6.6 being determined by the gate-drain distance.

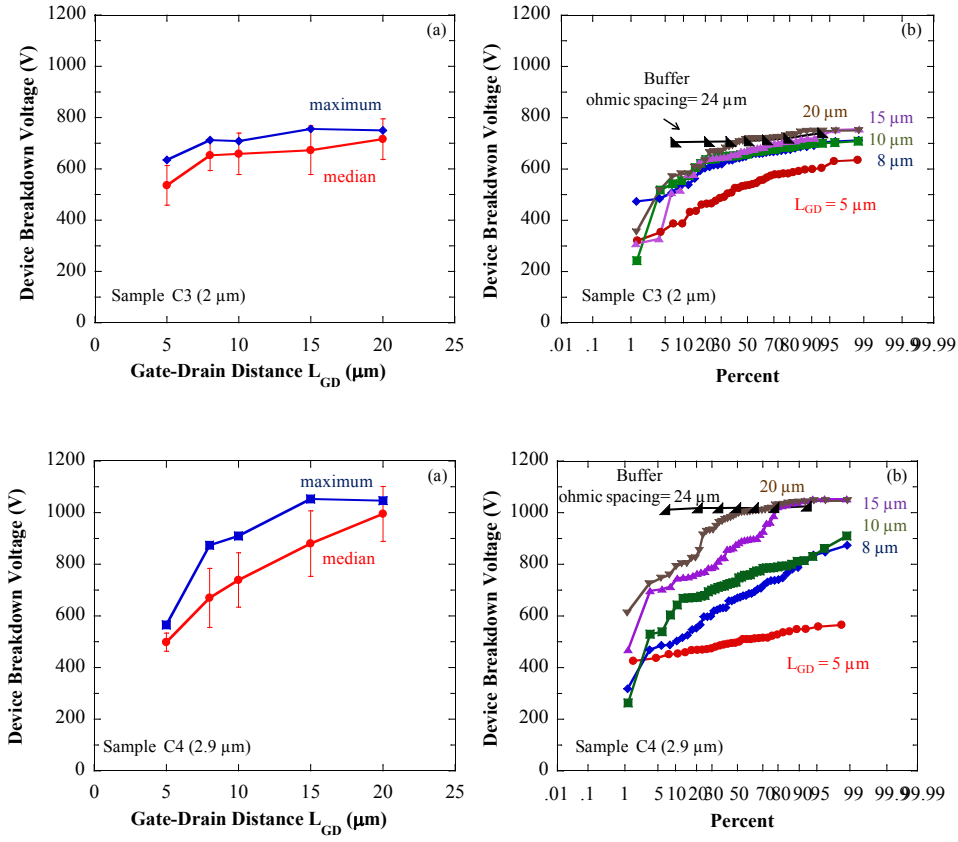


**Fig. 6.7** Device breakdown voltage in samples C3 (a) (b) and C4 (c) (d). The highest device breakdown voltage is comparable to the buffer breakdown voltage.

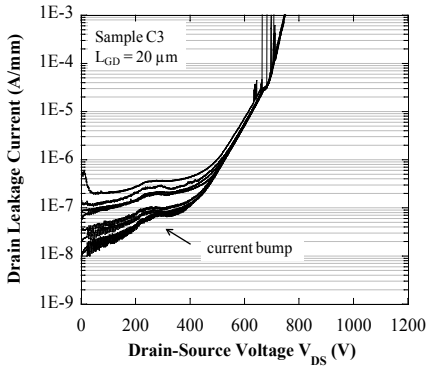


**Fig. 6.8** Drain leakage current measured in several transistors with $L_{GD}$=20 µm.

In conclusion, the device breakdown voltage saturates at a certain $L_{GD}$ at a value determined by the nitride buffer thickness. The growth of a thick buffer nitride layer is the most common technique to increase the breakdown voltage of GaN-on-Si devices. Ikeda *et al.* showed a device breakdown voltage as high as 2450 V with a specific on-resistance of 7 mΩ·cm$^2$ by using an AlN/GaN buffer structure as thick as 7.3 µm in combination with the C doping and the field plate technique.[4] However, the growth of such thick buffer layer on Si is challenging due to the large lattice and thermal mismatch between GaN and Si. In Imec the Si removal technique developed by Srivastava *et al.* [6,7,8] shows that after removing the Si substrate the breakdown voltage linearly increases with the gate-drain distance. Figure 6.9 shows the buffer and device breakdown voltage before and after complete removal of the Si substrate.[6] After completely removing the Si substrate the device breakdown voltage is as high as 1135 V for $L_{GD}$=15 µm compared to 750 V obtained in the same device with the Si substrate. Moreover, this technique works even if the Si substrate is locally removed only between source and drain ohmic contacts. A device breakdown voltage more than 2000 V was reached with only 2 µm buffer thickness and with $L_{GD}$ = 20 µm[7]. Recently, Srivastava *et al.*[8] show that the enhancement of the device breakdown voltage can be obtained using a Si Trench Around Drain Contacts (STAD) to electrically isolate the gate and the source contacts from the drain contact across the AlN/Si interface.

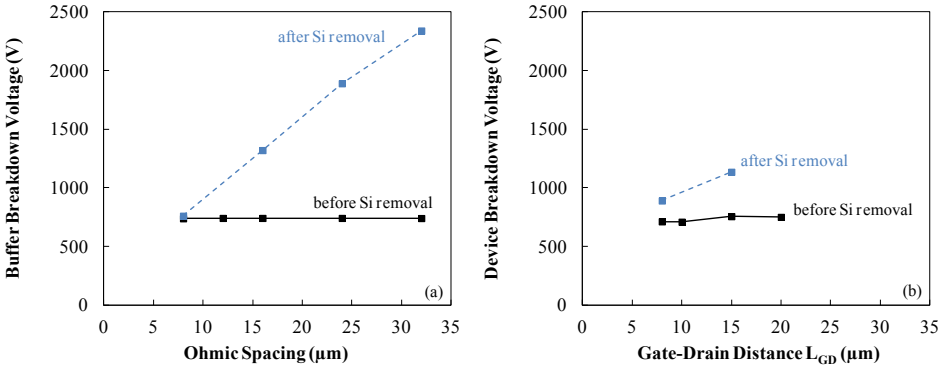


**Fig. 6.9** Buffer breakdown voltage (a) and device breakdown voltage (b) measured before and after complete removal of the Si substrate.[6]

On samples C3 and C4 we measured the on-resistance as we described in Chapter 4. The on-resistance, as expected, linearly increases with $L_{GD}$ and it is independent on the buffer thickness. Figure 6.10 shows the on-resistance distribution measured on 50 devices. From the median value we calculate the specific on-resistance ($R_{ON}$). The spread of each device geometry is less than 0.5 Ω·mm.

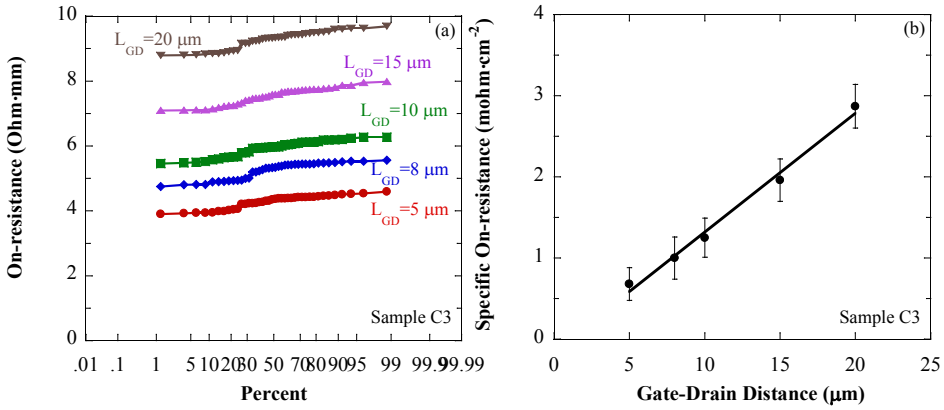


**Fig. 6.10** On resistance distribution (a) and specific on-resistance (b).

## 6.4 High voltage simulations of AlGaN/GaN HEMTs

We performed high voltage simulations of AlGaN/GaN devices with and without Si substrate. For comparison we also simulated AlGaN/GaN devices with the SiC substrate. Figure 3.2 in Chapter 3 shows the AlGaN/GaN used in the simulations. Figure 6.11 shows the device breakdown voltage and the off-state $I_{DS}V_{DS}$ curves simulated for a device with $L_{GD}$= 2 µm, 8 µm, 12 µm and 20 µm and 1 µm buffer thickness, with and without Si substrate. The simulated device breakdown voltage with and without Si substrate shows the same behavior as the electrical measurements. With the Si substrate the breakdown voltage simulated for different $L_{GD}$ saturates at about 680 V, while, in the same devices without Si, it linearly increases with $L_{GD}$. The electron density and the impact ionization factor extrapolated along the gate edge from the AlGaN surface down to the Si substrate are shown in Fig. 6.12. For devices without Si the channel depletes by increasing the drain voltage up to the breakdown regime and the electrons spread into the GaN buffer layer. In the structure with Si the electron density is higher in the substrate showing a peak at the Si interface as shown in Fig. 6.12a. This electron peak at the GaN/Si interface is due to the GaN spontaneous polarization induced charge which attracts electrons. Indeed, a similar peak is present even if we simulate the same structure with the SiC substrate.

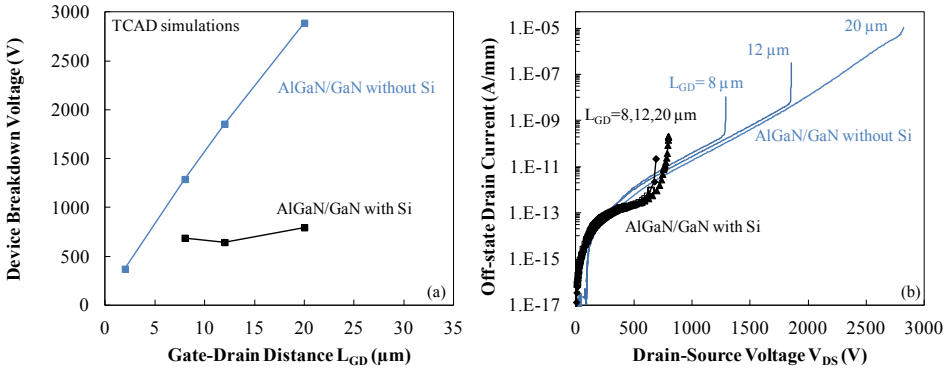


**Fig. 6.11** TCAD Simulations at high voltage of AlGaN/GaN SHFETs with and without Si substrate for different $L_{GD}$: device breakdown voltage (a) and off-state drain current at $V_{GS}$= -8 V (b).

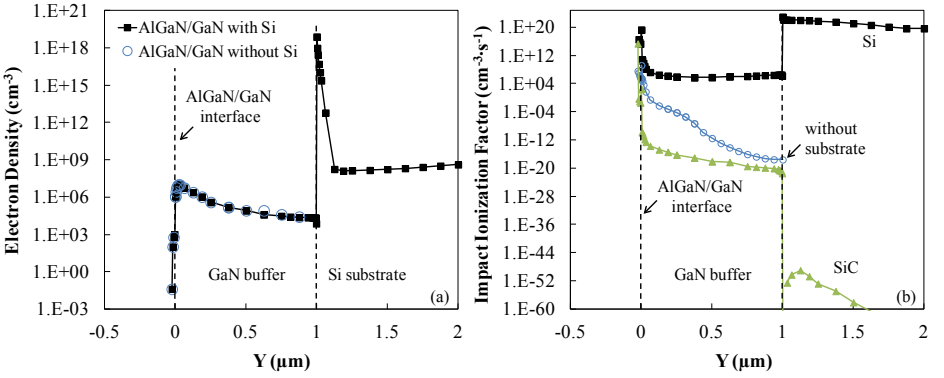


**Fig. 6.12** Depth profile of electron density (a) and impact ionization factor (b) in AlGaN/GaN SHFETs with Si and SiC substrate and without substrate.

However, this “channel” depletes much slower than the 2DEG creating a current path at the GaN/Si (or GaN/SiC) interface. The main difference with the device with SiC substrate is that the impact ionization factor is much higher at the GaN/Si interface compared to at GaN/SiC interface causing the breakdown at the Si interface (Fig. 6.12b). These simulations confirm that the lower critical electric field of Si limits the breakdown voltage of AlGaN/GaN devices.

## 6.5 AlGaN/GaN/AlGaN enhancement-mode device

AlGaN/GaN enhancement-mode (normally-off) devices are preferred for power switching because of their fail-safe nature and the circuit complexity reduction. Several different approaches have been demonstrated to make enhancement mode devices.[10-17] Oka and Nozawa demonstrated an enhancement mode AlGaN/GaN device with a threshold voltage as high as 5.2 V by using an AlGaN/GaN recessed MIS-gate HFET with a breakdown voltage of 400 V in a device with $L_{GD}$= 6.5 μm measured at zero gate voltage. However, the off-state drain leakage current is not low enough for power electronics applications.[11] Also the Fluorine treatment[12] and the introduction of a p-AlGaN layer[13] lead to positive threshold voltage. A MIS-HEMT structure with n-GaN/i-AlN/n-GaN triple cap layer in combination with a high-k gate dielectric is shown to be effective in providing enhancement mode operation with dispersion of less than 5% and a breakdown voltage of 320 V for a device with gate-drain distance of 5 μm.[14] The difficulty to make enhancement mode devices on AlGaN/GaN buffer layers is due to the spontaneous polarization induced charge at the AlGaN/GaN interface which make the AlGaN/GaN devices excellent natural depletion mode devices. Recently, it has been suggested to use non-polar m-plane GaN substrate because the non-polar planes do not induce polarization charge. Indeed, a positive threshold voltage of +3V is reached.[17] However, these devices are fabricated on GaN substrates which are extremely expensive. In this paragraph we not only describe our approach for the fabrication of e-mode devices but we also discuss the limitation of such devices in achieving high breakdown voltage. We show that the breakdown voltage of e-mode devices saturates at large gate-drain distance at a certain value determined by the nitride buffer layer structure. For a buffer thickness of 2 μm this value is around 700 V which is the same as for d-mode devices. This is a further confirmation that the breakdown voltage in GaN-on-Si devices is limited by the Si substrate and not by the device geometry.

In Chapter 2 we discussed the advantages of the *in-situ* SiN layer especially when it is grown on top of a thin AlGaN barrier layer.[18] Figure 6.13 shows the epilayer stack on the left. As for the depletion-mode, it based on the DHFET structure with the exception of a thinner AlGaN barrier layer. The total buffer thickness is 2 μm. The *in-situ* SiN layer preserves the 2DEG quality when scaling down the barrier thickness as shown in Fig. 6.14. This confirms the effectiveness of our in-situ grown SiN. The Si

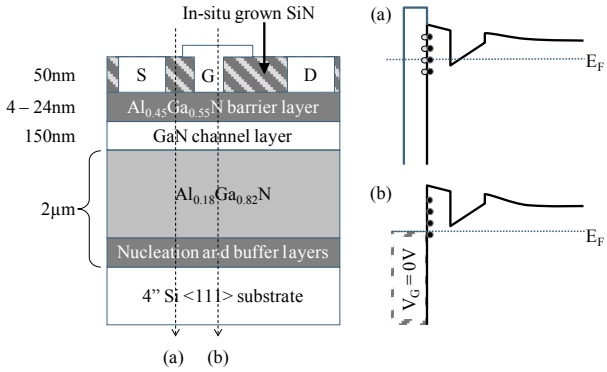


**Fig. 6.13** Schematic epilayer stack on the left and band diagrams on the right in the access areas (a) and under the gate for thin $Al_{0.45}Ga_{0.55}N$ barriers (b).

atoms act as surface donors donating electrons. By removing the *in-situ* SiN under the gate electrode prior to the gate metallization, we locally modify the AlGaN surface potential. As a result, the channel is depleted under the gate and thus e-mode operation is obtained as shown in Fig. 6.13. At the same time, low access resistance is maintained in the source-gate and gate-drain areas where the SiN remains (Fig. 6.13). The etching process of the AlGaN barrier layer is based on $SF_6$ chemistry. We optimized the process parameters of this etch to avoid implantation of $F^-$ ions under the gate. This is achieved by a reduction of the RF power during ICP etching from 50 W to 5 W. Figure 6.15a shows the impact of both the $Al_{0.45\%}Ga_{0.55\%}N$ top barrier layer thickness and the plasma etching conditions on the threshold voltage of the device. The high power etch facilitates enhancement mode operation by implantation of negatively charged fluorine ions that deplete the channel and shift the $V_T$ 1.5 V more positive. However, it has been shown that these ions are not stable under thermal stress causing a shift of the $V_T$ back to more negative voltages.[19] Based on these results, we focus only on the structure with 4 nm thick barrier layer that shows the most positive threshold voltage. An important feature of our approach is that the $V_T$ is mainly determined by the design and uniformity of the epitaxial layer stack and the devices' gate length. Fig. 6.15b shows the normalized histograms of the $V_T$ for the four different gate lengths used. Very narrow distributions for $V_T$ as function of the gate length are obtained.

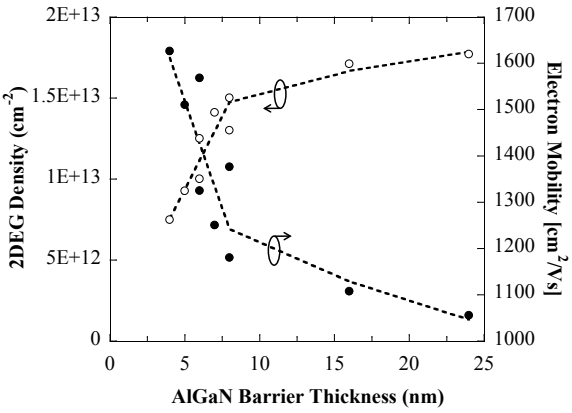


**Fig. 6.14** 2DEG density and associated mobility for different $Al_{0.45}Ga_{0.55}N$ barrier thickness with 50 nm of in-situ SiN passivation layer.

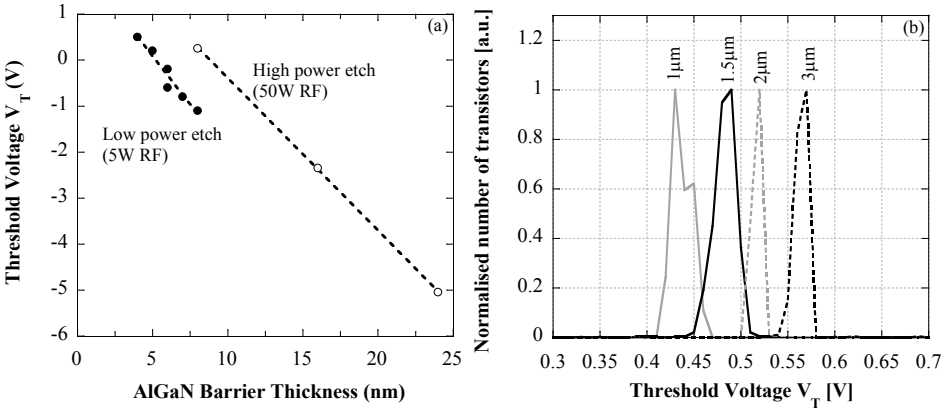


**Fig. 6.15** Threshold voltages as function of the AlGaN barrier thickness and RF power of the SiN plasma etch (a). Normalised distributions of $V_T$ for devices with different gate lengths on the wafer with the 4 nm $Al_{0.45}Ga_{0.55}N$ top barrier (b).

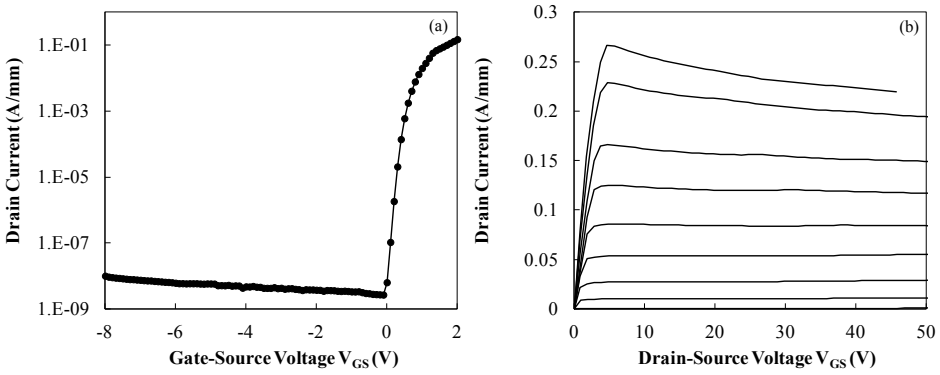


**Fig. 6.16** DC characteristics of a device with $L_G$ = 1.5 µm and $L_{GD}$= 8 µm: transfer curve (a) and output characteristics with $V_{GS}$ swept down from 2 V in 0.2 V steps (b).

This is in agreement with the sheet resistivity mapping on this wafer prior to processing that yields a standard deviation of only 1.98%. The typical transfer characteristic for devices with $L_G$ = 1.5 µm and $L_{GD}$ = 8 µm are shown in Fig. 6.16a. It has a pinch-off current below $10^{-8}$ A/mm at $V_{GS}$ = 0 V and $V_{DS}$ = 15 V. The $I_{DS}$-$V_{DS}$ curves are shown in Fig. 6.16b. The saturation current $I_{DS,SAT}$ at $V_{GS}$= 2 V is more than 0.25 A/mm. The extrapolated on-state resistance is 12 Ω·mm which translates into a low specific on-resistance of 2.4 mΩ.cm$^2$. These values are well within the state-of-the-art for enhancement mode devices. However, both current and resistance values are worse than for depletion mode devices shown in the previous paragraph. This is the result of the thin $Al_{0.45\%}G_{0.55\%}N$ top barrier layer and the use a Schottky diode as the gate electrode. The use of a Schottky contact limits the gate voltage swing we can apply. The high voltage drain leakage current at $V_{GS}$= 0 V for a device with $L_{GD}$=8 µm is shown in Fig. 6.17a. The device breakdown voltage is as high as 710 V and the drain leakage current at $V_{DS}$= 560 V is only 5 µA/mm. Moreover, the same current bump around 250 V is visible in the drain leakage current. The presence of this current bump is an indication of the same breakdown and current mechanisms as for the d-mode. A direct comparison of the device breakdown voltage between enhancement and depletion mode devices with an identical buffer structure, buffer thickness and device layout is shown in Fig. 6.17b. The

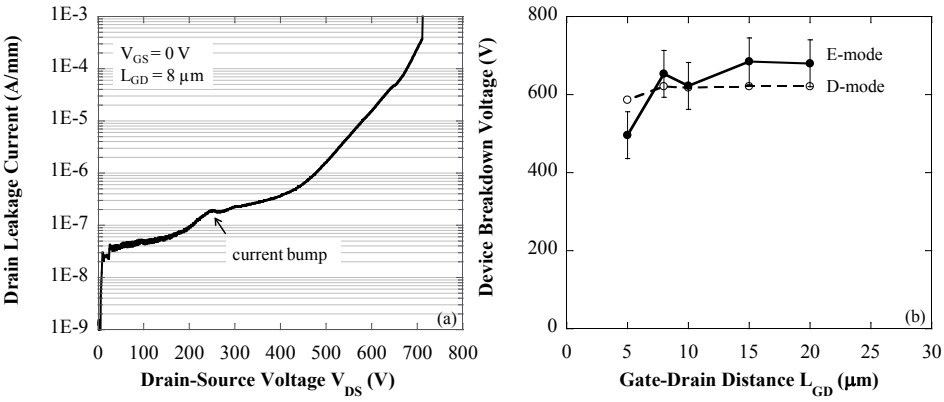


**Fig. 6.17** Breakdown curve measured at $V_{GS}$=0 V (a) and comparison between breakdown voltage of e-mode and d-mode devices for 2 µm buffer thickness (b).

device breakdown voltage saturates at $L_{GD}$= 8 µm at a value which is determined by the 2 µm nitride buffer layer thickness. Indeed, for both d-mode and e-mode devices with the same buffer thickness we found the same saturated breakdown voltage. Therefore, the same failure mechanisms as for d-mode devices can be identified. This is a further confirmation of the fact that it is the Si substrate the limiting factor in achieving high breakdown voltage in GaN-on-Si devices.

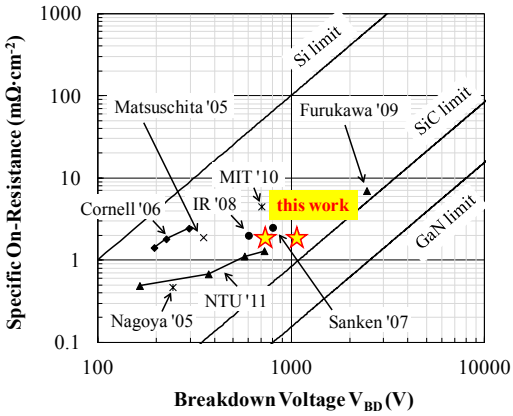


**Fig. 6.18** Specific on-resistance ($R_{ON}A$) versus the breakdown voltage ($V_{BD}$) for GaN-on-Si d-mode devices.

## 6.6 Specific on-resistance vs. breakdown voltage

The state-of-the-art in today's power switches is presented in terms of the specific on-resistance ($R_{ON}A$) vs. breakdown voltage ($V_{BD}$) as shown in Fig. 6.18. As explained in Chapter 1, this parameter links the conduction losses (on-state) and the device breakdown voltage (off-state). This parameter is an indication of how high the conduction losses are when the device operates in the on-state. Figure 6.18 shows an overview for depletion mode GaN-on-Si devices. For our devices, the specific on-resistance is about 2 mΩ·cm$^2$ independent of the buffer thickness. However, this value can be improved by reducing the device active area which has not been optimized. Selvaray *et al.*, from Nagoya Institute of Technology, worked on the optimization of thick buffer layers. They grew a buffer structure as thick as 9 µm formed by a thick GaN/AlN buffer layers followed by a thick GaN layer. They reached a device breakdown voltage as high as 403 V for $L_{GD}$=3 µm.[20] They did not provide the specific on-resistance so we couldn't include it in the graph above. International Rectifier showed a constant 800 V devices for $L_{GD}$= 11µm, 13µm and 18 µm.[21] Lu *et al.*, from The Massachusetts Institute of Technology, demonstrated a device breakdown voltage as high as 700 V with a specific on-resistance of 4.5 mΩ·cm$^2$ by using a Schottky

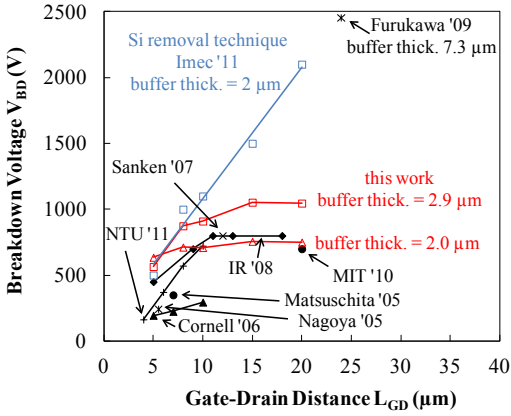


**Fig. 6.19** Device breakdown voltage as a function of the gate-drain distance in GaN-on-Si d-mode devices.

metallization in the drain contact.[22] Only Ikeda *et al.*, from The Furukawa Company, achieved a breakdown voltage as high as 2450 V with a specific on-resistance of 7 mΩ·cm$^2$ by using an AlN/GaN buffer structure as thick as 7.3 µm in combination with the C doping and the field plate technique.[23] Figure 6.19 shows the device breakdown voltage as a function of the gate-drain distance. A breakdown voltage as high as more than 1000 V is achieved in devices fabricated on a buffer thickness of only 2.9 µm. After the Si removal the breakdown voltage is comparable with the value achieved by The Furukawa Company but with the advantages of shorter gate-drain distance and, more important, very thin buffer layer.

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# Chapter 7

# Investigation Of The Leakage Current Bump

In this chapter we investigate the origin of the current bump measured in the leakage current of both device and isolation structures. We found that the bump appears when the structure is measured under ambient and microscope light and disappears if it is measured in the dark condition. Moreover, it reappears if the light is switched back on. We will show that this bump is due to an optically activated mechanism of charging and discharging of deep traps located at the Si interface. We first discuss the impurity states present at the Si interface such as Ga doping and $P_b$ defects, which make this interface highly conductive. Then, we will show the electrical and optical behavior under high electric field. Finally, we will explain the presence of the bump in the vertical measurements shown in Fig. 5.12.

## 7.1 Impurity states at the Si interface

In the previous chapters, we stated that the leakage current flows along the AlN/Si interface due to the high conductivity of this interface. This conductive path is created in the Si by the high Ga doping and the defect states near the interface.

### 7.1.1 Ga doping

The Ga acceptor doping occurs during the initial stage of the MOCVD growth. Due to the high background of Ga in the reactor from former growths, Ga is released during warming up and is diffused into the Si substrate. We carried out tests to reduce the effect of Ga doping experimentally by excluding GaN growth for a very long period by only growing AlN. From high frequency waveguide measurements we clearly could see a reduction in the absorption of the travelling wave. This was a clear indication of a lower conductivity of Si, showing smaller Ga doping. Moreover, we performed SRP measurements after nitride growing on highly resistive Si substrate. These measurements showed a doping density of more than $10^{17}$ $cm^{-3}$ at the Si interface decreasing into the substrate for a depth of 1 μm as shown in Fig. 7.1. Thus, there is a localized region near the interface where the Si resistivity drops while in the rest of the substrate remains unchanged.[1] This conductive channel causes parasitic losses degrading the high frequency RF performance. An optimization of the MOCVD growth led to a reduction of this parasitic doping of the Si substrate and consequently an improvement of the RF performance.[2,3]

### 7.1.2 Interface states

The defects that are created at the Si surface also happen during the first steps of growth. The high temperature destroys the crystalline layer forming amorphous centers. This has been shown by electron spin resonance (ESR) experiments. ESR measurements are performed in the as-grown samples shown in Fig. 7.2. Conventional first derivative absorption ($dP_\mu/dB$, where $P_\mu$ represents the incident microwave power) ESR spectra are measured at 4.2 K using a K band (~20.5 GHz) spectrometer driven in the adiabatic slow passage mode, as described elsewhere.[4] The signal anisotropy is analyzed by rotating the

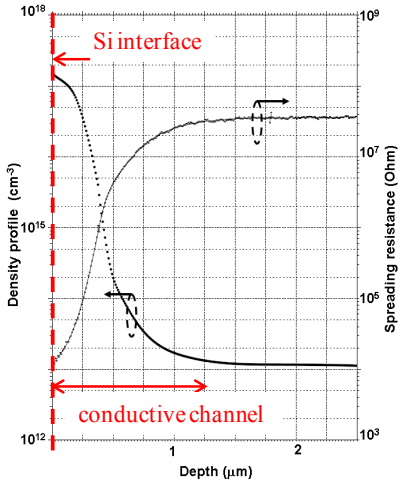


**Fig. 7.1** SRP characterization of Si. The Si resistivity drops near the interface and for a depth of 1 μm deep.[1]

applied magnetic field **B**, at angle $\varphi_B$ with the [111] sample normal **n,** in the $(1\bar{1}0)$ plane. Defect density and g value are determined relative to a co-mounted Si:P marker sample (g = 1.99869 ± 0.00002 at 4.2 K). Generally, two types of ESR signals are observed: one corresponds to the $P_b^{(111)}$ centers and the other to the D-line.

The $P_b$ center has been identified as[5,6,7] an interfacial Si dangling bond (DB), that is, interfacial $Si_3{\equiv}Si^{\bullet}$, where the dot represents an unpaired electron in a $sp_3$-type orbital. It represents the archetypal, and the only one observed by ESR, interface defect at the standard thermal (111)$Si/SiO_2$ interface. These intrinsic trivalent Si defects are inherently incorporated at the $Si/SiO_2$ interface to account for c-Si lattice –a-$SiO_2$ network mismatch. For standard oxidation temperatures (800-960 °C), a natural density of about $5 \times 10^{12}$ $cm^{-2}$ of physical $P_b$ defect sites is invariably incorporated.[4,8] This number includes both the ESR active defects –in the paramagnetic state–, and inactivated ones, e.g., passivated by hydrogen. Whereas only one type of $P_b$ center is observed at the standard thermal (111)$Si/SiO_2$ interface, the (100)$Si/SiO_2$ generally

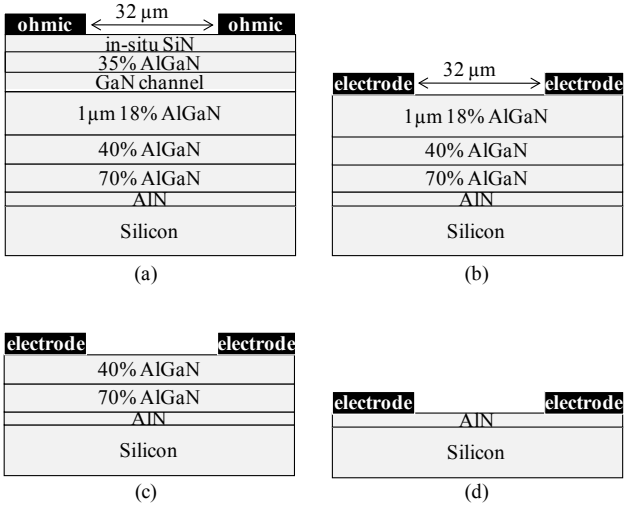


**Fig. 7.2** Standard buffer layer (a). Simplified buffer layer structures (b), (c) and (d).

exhibits two variants,[7] denoted as $P_{b0}$ and $P_{b1}$; the $P_{b0}$ variant is much similar to the $P_b$ center at the (111)Si/$SiO_2$ interface. Fortunately, these substantial systems of interface defects can be readily passivated by hydrogen[9,10] ($P_b$-H formation), the main goal of the commonly applied annealing in forming gas (10 % $H_2$ in $N_2$) in Si device technology. More specifically, as to the $P_b$ center in standard thermal (111)Si/$SiO_2$, only the variant with the Si DB ($sp_3$ orbital) axis directed along the [111] normal to the (111)Si/$SiO_2$ interface is occurring (observed by ESR), and which is pictured as pointing into the oxide layer. As illustrated in Fig. 7.3a, this defect is also observed here at the (111)Si/AlN interface, in densities of (1-3) $\times 10^{11}$ $cm^{-2}$. For the measurements with **B//n,** it corresponds to the ESR signal observed at zero crossing g value $g_c$=2.0014. More remarkable is the observation of the other variants of $P_b$ centers with the unpaired $sp_3$-orbital directed along the other crystallographically equivalent <111> directions, i.e.

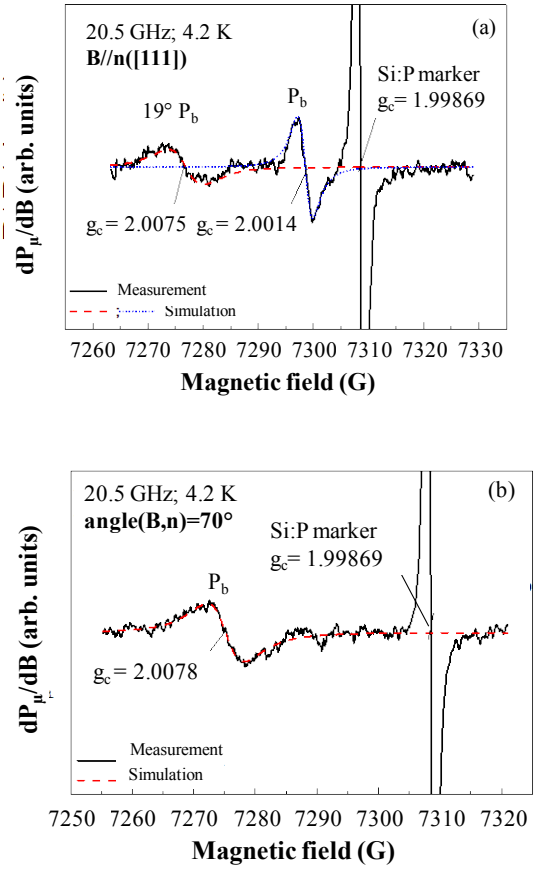


**Fig. 7.3** The ESR spectrum shows the presence of the regular $P_b$ and of the 19° $P_b$ centers (a). By $\overline{B}$ turning from $\overline{B}$ //n to the angle $\varphi_B = 70°$, the regular $P_b$ and the 19°ones coalesce into one signal (b).

$[\bar{1}11]$, $[1\bar{1}1]$, and $[11\bar{1}]$, at angle of about 19° with the (111)Si/$SiO_2$ interface, named 19° $P_b$ centers. In Fig. 7.3a, the 19° $P_b$ centers are at the origin of the signal at $g_c$=2.0075 and as expected, for $\overline{B}$ turning from the $\overline{B}$//n direction to the angle $\varphi_B$=70°, the regular $P_b$ centers and the 19° ones coalesce into one signal at $g_c$=2.0078. This is illustrated in Fig.7.3b, thus providing clear proof for the presence of the 19° $P_b$ centers. These have been reported once before[11], but only at (111)Si/$SiO_2$ interfaces denoted there as being of low quality. Their appearance may be seen as indicative of a less flat (corrugated) interface. If all four equivalent <111> Si DB directions would occur with equal probability, then for **B**//**n**, a value R=3 is expected for the density ratio of the 19° $P_b$ centers to the regular ones (Si DB directed along **n**). Within experimental accuracy, this indeed is the value observed in our samples, indicating all four possible interfacial Si DB directions occur in about equal probability. Figure 7.4 shows a schematic drawing of the 19° $P_b$ center at the (111)Si/$SiO_2$ interface together with the regular $P_b$ center.

Having identified and quantified these $P_b$-type centers, it is of much interest to address their electrical properties. From electrical measurements in conjunction with ESR, the regular $P_b$ centers have been shown to be amphoteric charge traps[12] of effective correlation energy $U_e$~0.5 eV, giving rise to two peaks of levels in the Si bandgap with corresponding +/0 and 0/- transition maxima situated at ~0.3 and ~0.8 eV above the Si valence band edge $E_v$ as Fig. 7.5 shows.[13] Unfortunately, the correlative electrical analysis-ESR study for the 19° $P_b$ variants has not been carried out. But there is little doubt that they give rise to typical $P_b$ energy trap levels in the band gap, and moreover, of much broadened distribution, tailing towards either band gap edge. This inference is hinted by various observations. For one, as shown before, a less quality (111)Si/$SiO_2$ interface is characterized by a $P_b$ defect distribution of enhanced spread in the activation energy $E_f$ for passivation in hydrogen[14], which is uniquely related with an enhanced spread of the defect levels in the bandgap.[4,14] At the interface, there is a configurational distribution in the $P_b$ centers, which is reflected in the energy level distribution.

Next, there is the ESR observation of the general presence of a second ESR signal, the D line[15,16] at $g_c$~2.0055. As identified before, it stems from unpaired Si DBs in an amorphous environment (viz., $P_b$-like centers in an amorphous Si matrix). It is the signal typically observed in a-Si layers, where, among others, the defects are at the origin of a substantial distribution of levels in the bandgap[15,16], including bandgap

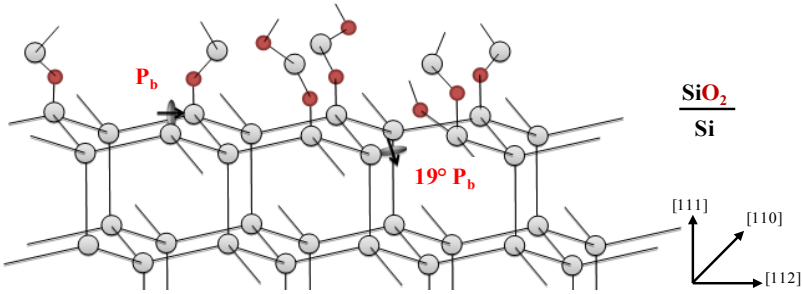


**Fig. 7.4** Schematic drawing of the regular $P_b$ and of the 19° $P_b$ centers at the Si interface.

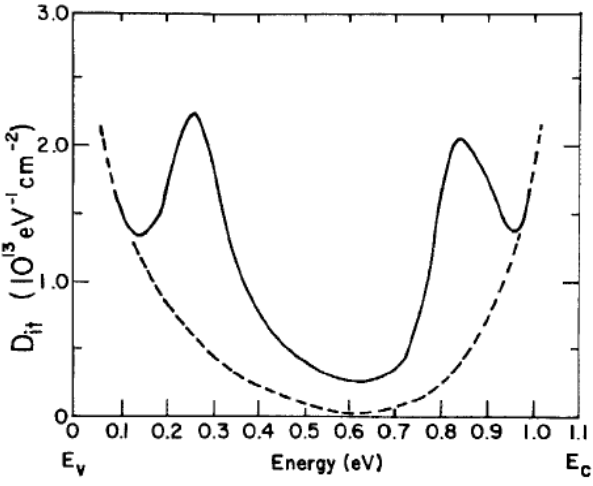


**Fig. 7.5** Bandgap distribution of interface trap density $D_{it}$ of $P_b$ centers. The two peaks are situated at 0.3 eV and 0.8 eV from the Si valence band, respectevely.[13]

tailing. Their presence will add to the trap level features introduced by the 19° $P_b$ centers.

Thus, all in all, the ESR data do indicate a low quality (111)Si/AlN interface in terms of occurring point defects, or at least, an interface of less ideal nature than a standard thermal $Si/SiO_2$ one. The (111)Si/AlN interface exhibits defect systems that give rise to band gap tailing together with a broad distribution of levels in the bandgap.

Therefore, we can conclude that these point defects and the high Ga doping play the role of creating an impurity band and tail states as shown in Fig. 7.6 and Fig. 7.7.[17] The extended states that are formed in this way can act as conductive channels. Therefore, the leakage current horizontally flows along the Si interface

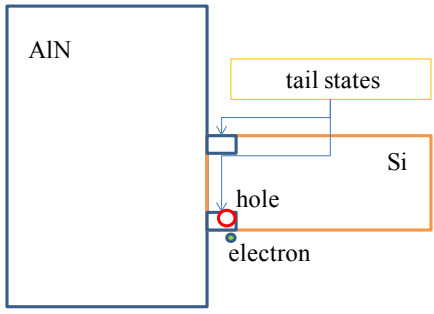


**Fig. 7.6** Schematic drawing of the deep traps levels and of the doping concentration in the Si top layer which create an impurity band and tail states.

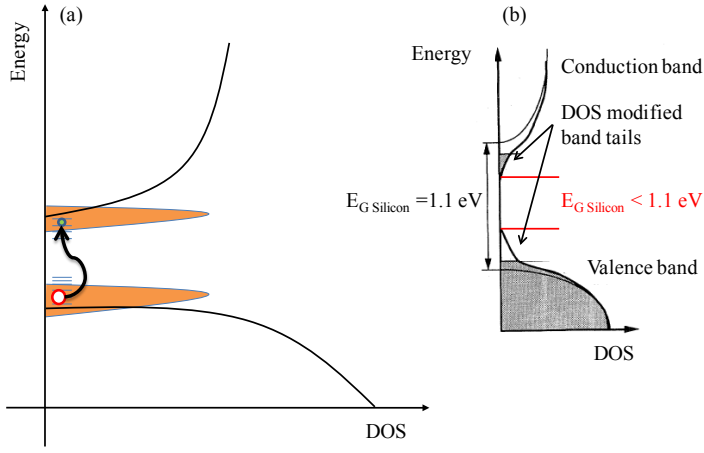


**Fig. 7.7** Schematic drawing of the density of states (DOS) created by the deep traps. The two peaks indicate the $P_b$ centers which are amphoteric. (a). The thin lines denote the unperturbed DOS while the thick lines depict the DOS modified by heavy-doping effect: both valence and conduction band are shifted towards each other (band gap narrowing) and the DOS is distorted showing band tails (b).[17]

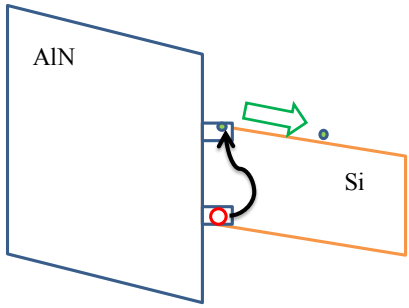


**Fig. 7.8** Schematic drawing of the band diagram with impurity bands under high electric field condition.

## 7.2 Permanent photoconductivity

As shown in Fig. 7.6 and Fig. 7.7, the created defect levels form deep traps and, lately impurity bands, which allow for continuous or hopping electron (or hole) transport. Near the band edges, the effective bandgap is lowered due to tail states as shown in Fig. 7.7b. When the sample is illuminated the light is absorbed by the Si layer even at frequencies lower than the pure Si band gap near the interface due to the reduced bandgap. The acceptors can be negatively charged with an electron. Upon light absorption, the electron will be excited to the conduction impurity band leaving behind a neutral acceptor and an excited electron in an extended state (Fig. 7.7a). Most likely, the hole can also move to generate a positive current. The charges reside in a kind of well in long living states, giving rise to almost permanent photoconductivity. Indeed, the lifetime of these charges in the tail states is relatively long, and photoconductivity can last for minutes. This behavior changes when an electric field is applied by biasing the heterostructure. When the applied electric field is high enough, the charges can escape and the photoconductive effect disappears (Fig. 7.8).

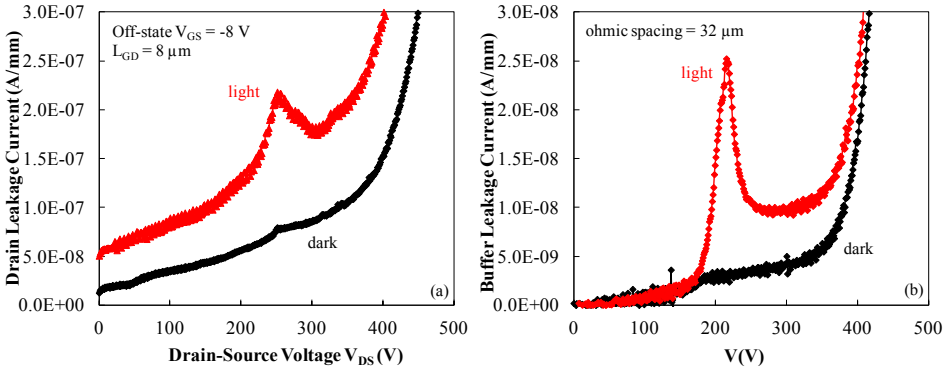


**Fig. 7.9** OFF-state I-V measurements under ambient and microscope light, and in the dark conditions. Device leakage current (a). Buffer leakage current (b).

## 7.3 Electrical behavior of the current bump

In the previous chapters we showed the current bump in the leakage current of both the device and isolation structure. Figure 7.9a shows the drain leakage current of a standard transistor with gate-drain distance ($L_{GD}$) of 8 µm. Figure 7.9b shows the buffer leakage current in an isolation structure with 32 µm ohmic spacing. When the I-V measurement is performed under ambient and microscope light a current bump is observed between 150 V and 300 V. The bump is not detected if the light is switched off. An important feature of this bump is that it does not affect the breakdown voltage. Figure 7.10 shows that the same breakdown voltage is measured in the isolation structure for both light on and off conditions. However, the leakage current measured in the dark condition is one order of magnitude lower than the leakage current measured with the light on in the voltage range from 250 V up to almost 400 V. When the light is on and the electric field is high enough, the electrons excited and accumulated in the extended states can escape contributing to the leakage current as a bump. When the electric field increases, the electrons immediately escape as soon as they reach the impurity state. This explains the higher leakage current between 250 V and 400 V compared to the leakage current with the light off.

In order to identify the origin of this bump we simplified the epilayer structure by growing the buffer layer stack only up to the $Al_{0.18}Ga_{0.82}N$ buffer layer, only up to the $Al_{0.40}Ga_{0.60}N$ and only up to the AlN as shown in Fig. 7.2b,c and d, respectively. The processing is limited to the formation of two unalloyed electrodes and the metal stack used is 10 nm TiW/160 nm Au. Also these simplified epilayer stacks show the current bump under illumination. No bump is detected if the light is switched off. Therefore, we can exclude that the origin of the bump is related to traps at the AlGaN surface, in the SiN passivation layer, in the channel or in one of the nitride buffer layers. The fact that the bump is measured in the layer stack with only the AlN on top of Si points to the AlN/Si interface. Indeed, the bump disappears if the Si substrate is removed. Figure 7.11 shows the I-V characteristic measured with the light on after removing the Si substrate in the standard buffer layer shown in Fig 7.2a. However, to better understand the electrical behavior of the current bump we performed several experiments.

In the first experiment we studied the reproducibility of the bump. On the same isolation structure we performed several consecutive measurements alternatively switching the light on and off as shown in Fig. 7.12. The first measurement is performed with the light on (blue curve). The bump disappears if the light is switched off (black curve) and reappears with the same area (red curve) as in the first measurement if the light is switched back on. Before performing this last measurement (red curve) we need to wait about 30-40 minutes to find the same bump. This is an indication of deep traps. Moreover, the same behavior is found if the first measurement is done with the light off. In the second experiment, we consecutively applied forward and reverse voltage sweeps up to 300 V and backwards, respectively. Fig. 7.13a shows both forward and reverse voltage sweeps. During the reverse sweep the current bump is not detected. Moreover, after consecutive forward and reverse sweeps, performed on the same isolation structure, the area under the bump saturates as shown in Fig. 7.13b. The fact that the bump is not present during the reverse sweep can be explained considering the fact that the electrons excited in the impurity band immediately escape due to the high electric field.

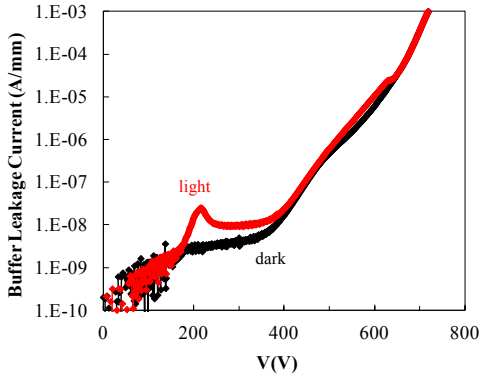


**Fig. 7.10** The current bump does have an impact only on the leakage current in the range of 250 V up to 400 V. The breakdown voltage is the same for both conditions.

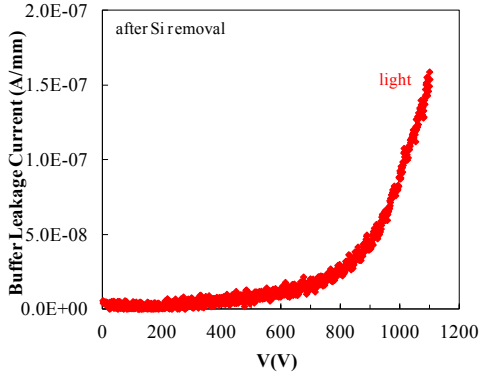


**Fig. 7.11** Buffer leakage current measured under ambient and microscope illumination after removing the silicon substrate in the structure of Fig. 7.2a.

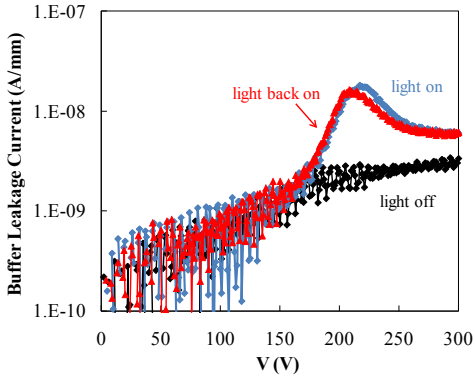


**Fig. 7.12** The blue curve is the first measurement and it is done with the light on. The current bump disappears (black curve) and reappears (red curve) if the light is switched off and back on, respectively. The area under the bump is the same for both the red and blue curves.

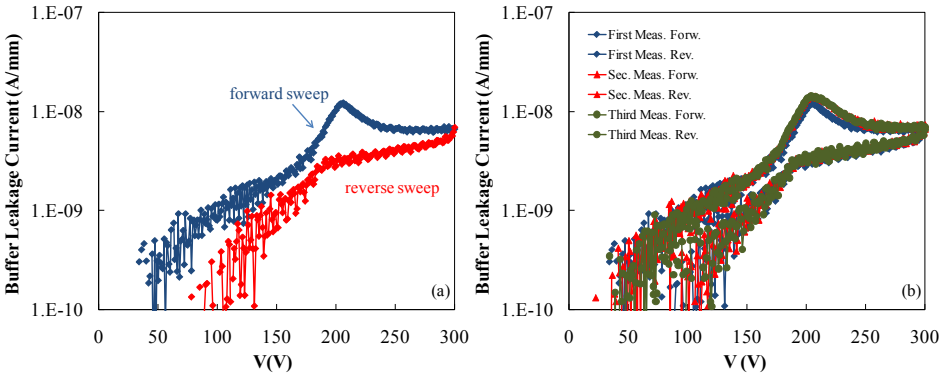


**Fig. 7.13** Forward and reverse sweep performed on the same isolation structure (a). Three consecutive measurements performed on the same isolation structure show that the area under the bump saturates (b).

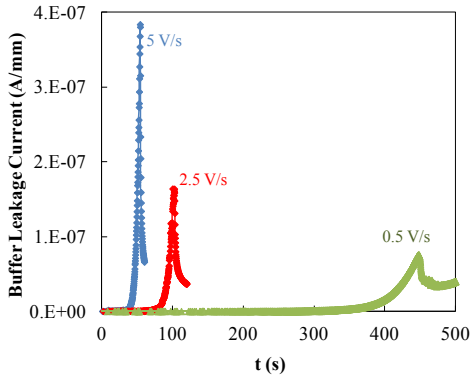


**Fig. 7.14** Buffer leakage current measured with three different voltage ramp rates.

### 7.3.1 Current bump versus ramp rate

We studied the behavior of the bump as a function of the ramp rate of the voltage applied. The voltage applied was swept from 0 V up to 300 V with the voltage ramp rates of 5 V/s, 2.5 V/s and 0.5 V/s. Figure 7.14 shows that by decreasing the voltage ramp rates the current bump appears after 30 s, 60 s and 300 s which correspond to a voltage as high as 150 V. The area under the bumps is approximately the same. These facts indicate that the amount of charge responsible for the bump and the electric field at which the bump starts appearing do not change with the measurement conditions.

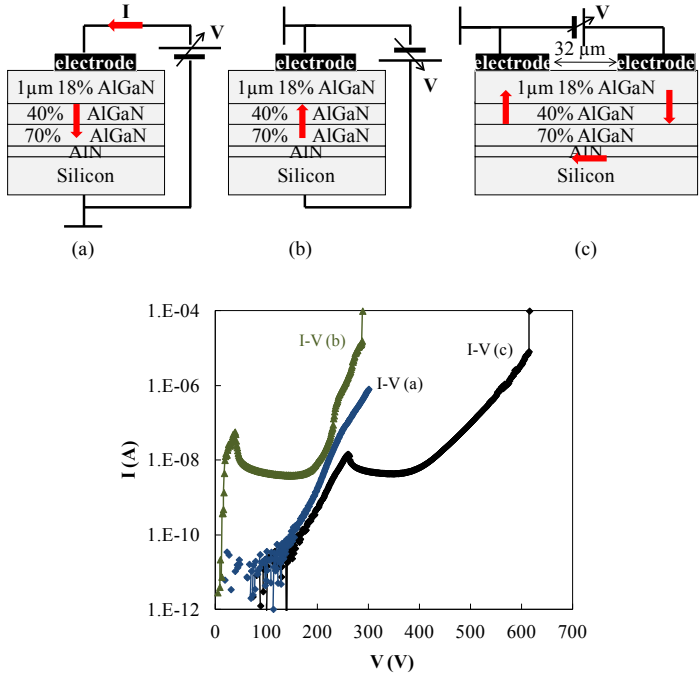


**Fig. 7.15** High voltage I-V characteristics measured in the vertical configurations showed in (a) and (b) and in the horizontal configuration showed in (c).

### 7.3.2 Current bump in vertical high voltage measurements

As we showed in Chapter 5, the buffer leakage current is also measured in the vertical direction in two configurations as Fig. 7.15 shows. In the configuration (a) the bias is applied on top of the buffer on the metal electrode and the Si substrate is grounded. In the configuration (b) the bias is applied directly to the Si substrate. In the measurement configuration (c) the buffer leakage current is measured between two neighboring metal top electrodes with the Si substrate floating. The I-V characteristics are shown in the plot of Fig. 7.15. It is clear that the leakage current measured in the configuration (c) is a combination of the vertical leakage currents measured in (a) and

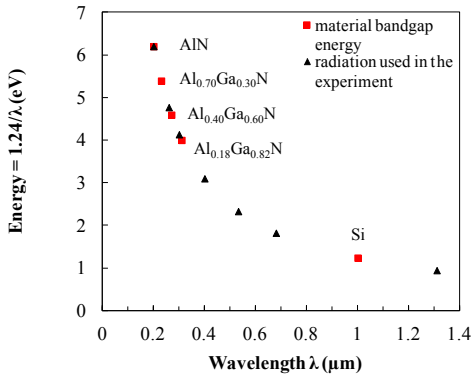


**Fig. 7.16** Relationship between energy and wavelength of the light sources used in the experiment (dark symbols). The bandgap energy of the nitride buffer layers and the Si substrate are also plotted (red symbols).

(b). However, the bump appears only when the Si substrate is biased as in (b). Indeed, in the case (a), the electrons, moving vertically from the Si to the metal electrode, "see" a big barrier due to the AlN layer and therefore cannot contribute to the current.

## 7.4 Optical behavior of the current bump

We investigated the spectral sensitivity of this bump by performing I-V characterization using light sources with different wavelengths. We measured the buffer leakage current while the isolation structure is exposed to light sources with different wavelengths, in the range of ultra violet, visible and infrared. We used seven different wavelengths: λ= 200-260-300-400-532-680-1310 nm. The radiation is produced by a 150 W Xe lamp with filters for wavelengths between 200 and 400 nm with an output power density of several μW/cm$^2$. For the wavelengths of 532 nm and 680 nm, which correspond to the green and red visible light, we used commercially available laser pointers with an output power of several mW. For the longest wavelength (1310 nm) we used a Mitsubishi laser diode with an output power of 5 mW. For λ= 200 nm only the AlN nucleation layer is transparent. For wavelengths longer than λ= 400 nm all nitride layers are transparent. For the longest λ all the layers, including the Si substrate, are

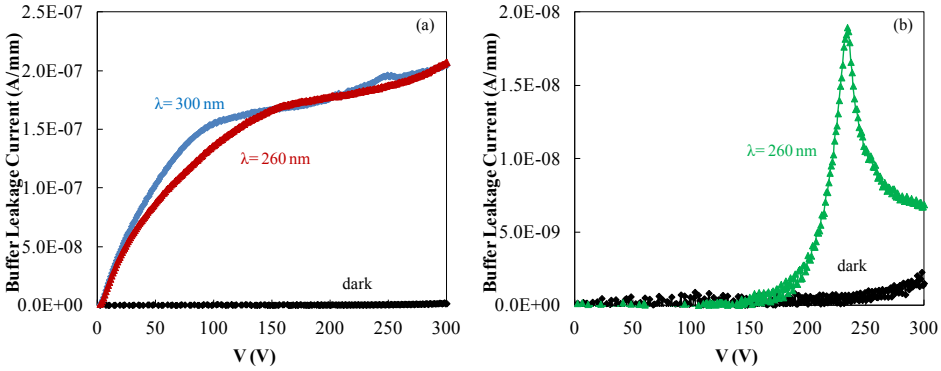


**Fig. 7.17** High-voltage buffer leakage current measured in the dark and under illumination with light of wavelength: λ= 260-300 nm (a) and λ= 532-680 nm (b).

transparent. Figure 7.16 shows the well known relationship between the wavelength and the corresponding energy of the radiation. For sake of clarity, we also plotted the bandgap energy of the AlGaN buffer layers and of the Si substrate. Figure 7.17 shows the high-voltage I-V curves measured on the same structure exposed to light with different wavelengths. The initial condition is the I-V measured in the dark where no traps are excited and the current level is $< 10^{-9}$ A/mm. After each measurement done under illumination we switched off the light and needed to wait for about 30-40 minutes in order to restore the initial condition. The fact that such long recovery time is needed is an indication for deep traps. The I-V measurements performed under illumination with λ= 260-300 nm are shown in Fig. 7.17a. The same behaviour is obtained for λ= 200 nm. The absorption of light with energy larger than the bandgap of the $Al_{0.18}Ga_{0.82}N$ layer generates a photoconductive path in the top layer hiding the current bump seen at longer wavelengths. For wavelengths longer than 300 nm all the layers, except Si, are transparent. Figure 7.17b shows the buffer leakage current measured under λ= 532 nm (2.33 eV) exposure where the current bump is clearly visible. The same behaviour is obtained with λ= 400 and 680 nm. When we use a photon source of λ=1310 nm (0.95eV) the Si substrate is also transparent. The current bump is however still present but the area under the bump is much smaller as compared to the previous measurements. We

conclude that the traps are not limited to a single energy level but are spread over an energy distribution. The energy of 0.95 eV is sufficient to excite most but not all the trap levels at the Si interface.

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# Chapter 8

# Summary, Conclusions and Outlook

This chapter summarizes the main results and achievements obtained during this Ph.D. project. Also, suggestions for future work, based on the present work, are given.

## 8.1 Summary and conclusions

This thesis has focused on the optimization of GaN-on-Si HEMTs for high voltage applications. GaN-on-Si technology is emerging as the best candidate to replace the well established Si technology due to the higher critical electric field, larger bandgap energy, higher electron mobility and higher saturation drift velocity of III-nitride materials compared to Si. Therefore, III-nitride materials are attractive for high-frequency, high-power, high-voltage, high-temperature and low-loss operating specifications as we discussed in **Chapter 1**.

In **Chapter 2** we described the physics of both AlGaN/GaN SHFET and AlGaN/GaN/AlGaN DHFET devices based on the piezoelectricity of the nitride materials which makes these devices naturally depletion mode.

TCAD simulations, described in **Chapter 3**, show that the main problem of these devices is the high electric field peak at the gate edge at the drain side in pinch-off condition. This electric field peak increases with the drain bias causing the device breakdown. The field plate technique is shown to be effective in reducing this peak allowing higher breakdown voltage. Also, we used the simulations to optimize the layer structure of the DHFET based devices in terms of GaN channel thickness and Al content of the AlGaN buffer layer. We found that with a GaN channel thickness of 150 nm and 18 % of Al concentration in the AlGaN buffer layer the electrons are well confined in the channel due to a higher conduction band profile. This is effective in reducing the buffer leakage current. Also, the critical electric field of the buffer layer is increased by the use of the AlGaN buffer layer compared to the GaN layer of the SHFET.

**Chapter 4** describes the dedicated mask for testing the impact of the device geometry on breakdown voltage. Also, the isolation structures for testing the buffer breakdown are described. The processing of our devices is described with particular attention to the isolation step. For both mesa etching and N implantation techniques, we optimized the conditions for a deep and shallow isolation.

In **Chapter 5** we presented the study done for the optimization of the buffer layer structure for high breakdown voltage. The breakdown mechanisms are identified and

addressed. High voltage measurements performed on buffer layers grown on both highly resistive (FZ) and highly conductive (CZ) Si substrate show the same results. The buffer breakdown voltage linearly increases for short ohmic spacing being dependent on the structure geometry. FIB images show that the breakdown occurs in the AlGaN buffer layer. For large ohmic spacing, the buffer breakdown voltage saturates at a value determined by the nitride buffer layer thickness. Indeed, increasing the thickness of the buffer layer the buffer breakdown voltage increases. FIB images of structures with large ohmic spacing show that the structure breaks in the Si substrate, most likely at the Si interface where, due to the roughness of the interface, the electric field distribution is not homogeneous. We also showed that the deep isolation lowers the leakage current at high voltage leading to high breakdown voltage. Another effect of the deep isolation is the saturation of the breakdown voltage even for the small ohmic spacing. The N implantation is found to reduce the leakage current more than the mesa etching due to a better protection of the surface from impurities and processing damages. The breakdown voltage obtained with the deep N implantation is slightly higher than the one obtained with the deep mesa etching. We also performed high voltage measurements in the vertical direction. They show a breakdown voltage a factor two lower than the horizontal one. This is due to a vertical double leakage current path from the ohmic contact into the Si substrate and a horizontal leakage current along the AlN/Si interface which cause a premature breakdown due to the inhomogeneous electric field distribution and to the low Si critical electric field. This explains the saturation of the breakdown voltage independently of the structure geometry. The use of a thick nitride layer, the deep N implantation and the high Al content of the AlGaN buffer layer only increase the saturated buffer breakdown voltage.

**Chapter 6** discusses the main results obtained in DHFET based devices. The device breakdown voltage shows the same behavior as the buffer. The devices are measured in the off-state with the Si substrate floating. For short gate-drain distance, the breakdown voltage linearly increases being dependent on the device geometry. More specifically, it is dependent on the electric field peak at the gate edge. Indeed, the use of an optimized field plate increases the breakdown voltage by more than a factor 2. For long gate-drain distance, the device breakdown voltage saturates at a value determined by the nitride buffer layer thickness. Indeed, the increase of the buffer layer thickness allows higher saturated breakdown voltage. The use of the field plate improves the

saturated breakdown voltage by only 10 %. Moreover, the same measurements performed with the Si substrate grounded show a value a factor two lower than the value measured with the Si floating. Therefore, the breakdown mechanisms in the devices are the same as in the buffer structures. The drain leakage current has an additional component which consists of a double leakage current from the ohmic contacts into the substrate and along the Si interface making the device breaking at the Si interface due to the lower critical electric field of Si compared to the nitride layers. We also show enhancement mode devices fabricated on the DHFET buffer layer. We realized normally off operation by thinning the AlGaN barrier layer and removing the *in-situ* SiN only below the gate. However, the most important result is that the breakdown voltage of e-mode devices shows the same behavior as of depletion mode devices. Therefore, we can conclude that the limiting factor of GaN based devices fabricated on buffer layers grown on Si substrate for high voltage applications is the Si substrate itself. High voltage simulations of AlGaN/GaN devices with and without Si substrate qualitatively confirm the electrical measurements. The simulations of AlGaN/GaN/Si devices with different gate-drain distance show the saturation of the breakdown voltage due to an electron path at the Si interface where the impact ionization factor is higher. Therefore, to linearly increase the breakdown voltage with the gate-drain distance of GaN-on-Si devices, we propose the Si trench around the drain contact in order to break the horizontal leakage path at the Si interface.

The buffer leakage current and the off-state drain leakage current show a current bump at high voltage. In **Chapter 7** we studied the optical and electrical behavior of the current bump by performing several experiments. We found that the bump appears when the structure is measured under ambient and microscope light and disappears if it is measured in the dark condition. Moreover, it reappears if the light it is switched back on. I-V measurements performed with different voltage ramp rates show that the slower the voltage sweep the later the bump appears. The corresponding voltage as well as the area under the bump does not depend on the ramp rate. We also investigated the spectral sensitivity of this bump by performing current-voltage (I-V) characterization using light sources with different wavelengths in order to identify from which layer the current bump is originated. We observed that the bump appears even if the sample is illuminated by photons with 0.95 eV energy for which all nitride buffer layers and the Si substrate are transparent. Only when the Si substrate is removed the bump is not observed. This

indicates that the current bump is due to an optically activated mechanism of charging and discharging of deep traps located at the Si interface. The Si top layer is highly p doped due to Ga diffusion and $P_b$ Si dangling bonds which play the role of creating an impurity band and tail states shrinking the Si band gap. The extended states that are formed in this way can act as conductive channels. Upon light absorption, the electron will be excited to the conduction impurity band leaving behind a neutral acceptor and an excited electron in an extended living state giving rise to a permanent photoconductivity. When the applied electric field is high enough, the excited and accumulated electrons escape and contribute to the leakage current with a bump.

## 8.2 Outlook

Despite the fact that Si is identified as the limiting factor for achieving high breakdown voltage, it may be possible to grow "tricky" buffer layer structures in order to electrically isolate the buffer from the Si substrate and, therefore, avoiding the saturation of the breakdown voltage without the need of removing the Si substrate. Certainly, the growth of the AlN nucleation layer on top of Si substrate is a key issue for high voltage operations.

Also, the active area of our devices is not optimized yet. Therefore, it is still possible to decrease the specific on-resistance without affecting the breakdown voltage.

Since switching applications require low gate leakage currents at high drain bias, the use of a gate dielectric is the best technique for decreasing the gate leakage current. However, the process of this layer is challenging from a dispersion point of view since another interface is added. Therefore, the electrical characterization of this interface is very important for studying its impact on switching performance. Also, the optimization of the gate dielectric deposition and the pre- and post- treatments such as cleaning and thermal annealing are crucial. So far, only a few publications report negligible dispersion.

From an enhancement mode operation point of view, a positive threshold voltage ($V_{th}$) of over +3 V is desired to ensure minimal subthreshold conduction. The subthreshold behavior is important because it determines off-state leakage currents. To

obtain low off-state leakage currents, devices must be completely turned off at gate-source voltage of 0 V. The reason for such a demanding requirement is that orders of magnitude of leakage current are controlled by small changes of gate-source voltage in the subthreshold slope region. However, the use of a thin AlGaN barrier layer together with a gate dielectric can lead to more positive threshold voltage together with low gate leakage at forward gate bias. Another important requirement is the large gate voltage swing. So far, the use of a Schottky gate has limited the forward gate voltage swing.